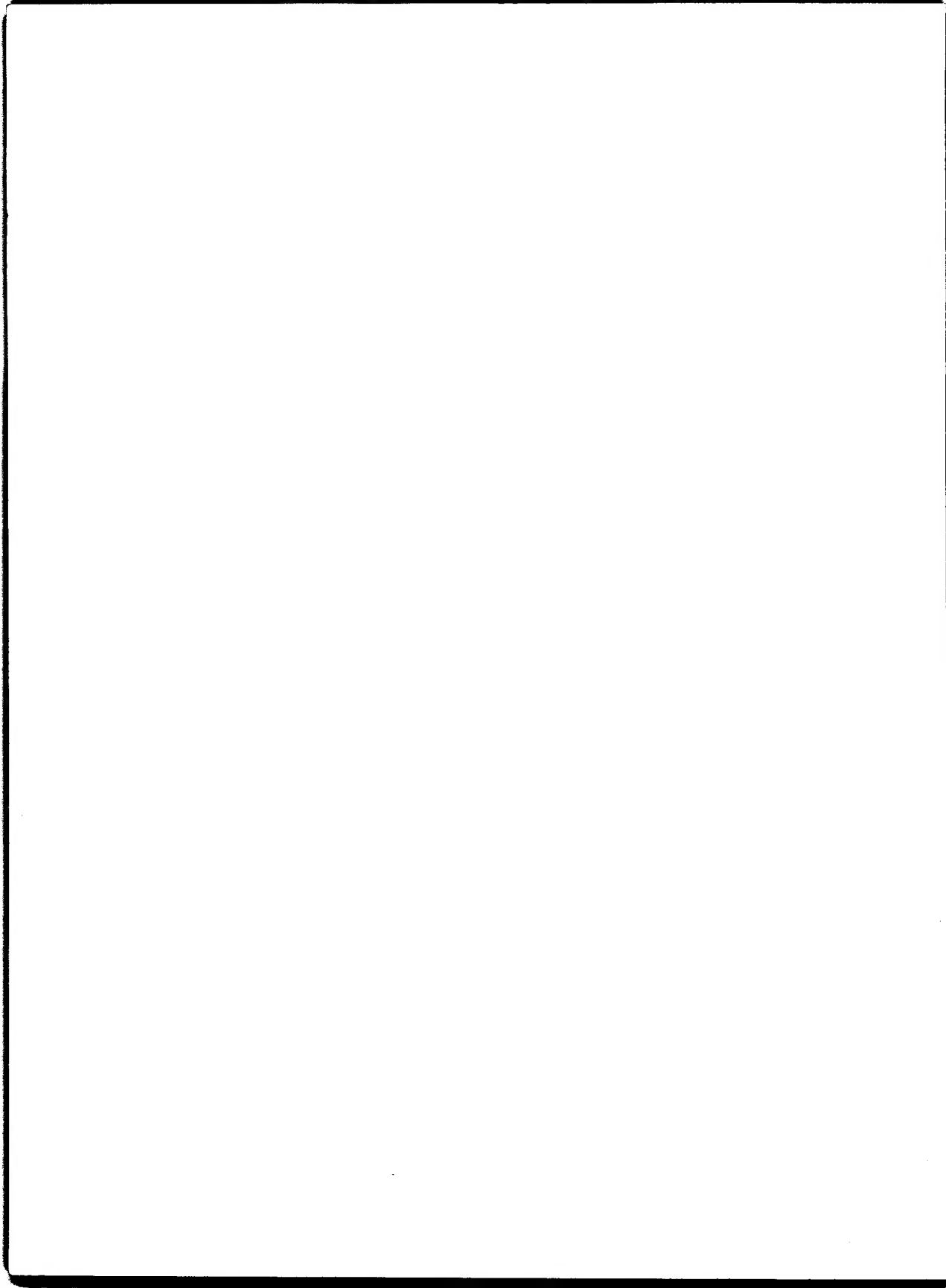
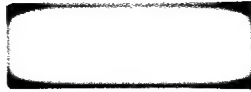


SONY®

Semiconductor IC

Data Book 1992 Memories





Semiconductor Integrated Circuit Data Book 1992

**List of Model Names/
Index by Usage**

1

Description

2

Static RAM

3

**Application Specific
Memories**

4

Mask ROM

5

Nonvolatile Memories

6



Semiconductor Integrated Circuit Data Book

1992

SONY®

PREFACE

This is the 1992 version of the Sony semiconductor IC data book. This book covers all the semiconductor products manufactured and marketed by Sony.

In preparation of this data book, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write; we welcome suggestions and comments.

Sony reserves the right to change products and specifications without prior notice.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

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Sony Semiconductor Data Books

The following data books are available for the respective products applications.

1. TV Devices
2. Video Recorder ICs
3. CCD Image Sensors & Peripheral ICs
4. Compact Displayer ICs
5. Digital Audio ICs
6. Analog Audio ICs
7. Floppy Disk/Hard Disk Drive ICs
8. Radio Communication System ICs
9. A/D, D/A Converters
10. ECL Logic/ASSP ICs
11. Microcomputers
12. Memories
13. Discrete Semiconductors
14. Laser Diodes

In addition, a List of Semiconductor Products covering all manufactured device on the market, is issued twice a year.

Data books offer information pertaining to the listed products.

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3) Mounting method	19
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1) Static RAM	27
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4) Nonvolatile Memories	399

1. List of Model Names

Type	Page	Type	Page	Type	Page
CXK5863AP/AJ	50	CXK58258AP/AJ	171	CXK581120J	323
CXK5863P/M/J	40	CXK58258BP/ BJ/BM	178	CXK584000TM/ YM/M/P	330
CXK5863BP/ BM/BJ	57	CXK58267AM	185	CXK584001TM/ YM/M/P	340
CXK5864BP/ BSP/BM	30	CXK58267ATM/ AYM	196	CXK7701J	351
CXK5866P/J	65	CXK59288P/J	207	CXK77910J	366
CXK5466P/J	72	CXK59289P/M	214	CXK384000	377
CXK5467P/J	80	CXK59290M/TM	221	CXK384001	384
CXK5971AP/ AM/AJ	88	CXK581000P/M	232	CXK388000	391
CXK5971P/M/J	96	CXK581000P/ M-□□□□ X	243	CXK1023P/M	401
CXK5972P/J	106	CXK581000P/ M-12LB	252	CXK1024P/M	409
CXK58257AP/ ASP/AM	113	CXK581001P/M	263	CXK27C256DQ	420
CXK58257ATM/ AYM	123	CXK581100TM/ YM	273	CXK27C512DQ	430
CXK58257ATM/ AYM-□□□□ X	143	CXK581100TM/ YM-□□□□ X	284	CXK27C1000DQ	441
CXK58257AP/ AM-□□□□ X	133	CXK581100TM/ YM-12LB	293	CXK27C1001DQ	451
CXK58257AP/ AM-12LB	153	CXK581020SP/J	304		
CXK58257ATM/ AYM-12LB	162	CXK581021J	313		

2. Index by Usage

1) Static RAM

Type	Memorie capacity	Functions	Access time	Page
CXK5864BP CXK5864BSP CXK5864BM	64k bit	8k×8bit	70/100/120ns	30
CXK5863P CXK5863M CXK5863J	64k bit	8k×8bit	25/30/35ns	40
CXK5863AP CXK5863AJ	64k bit	8k×8bit	20/25/30ns	50
CXK5863BP CXK5863BJ CXK5863BM	64k bit	8k×8bit	25/30/35ns	57
CXK5866P CXK5866J	64k bit	8k×8bit	15/20ns	65
CXK5466P CXK5466J	64k bit	16k×4bit	15/20ns	72
CXK5467P CXK5467J	64k bit	16k×4bit, \overline{OE} pin	15/20ns	80
CXK5971AP CXK5971AM CXK5971AJ	72k bit	8k×9bit	25/30/35ns	88
CXK5971P CXK5971M CXK5971J	72k bit	8k×9bit	25/30/35ns	96
CXK5972P CXK5972J	72k bit	8k×9bit	15/20ns	106
CXK58257AP CXK58257ASP CXK58257AM	256k bit	32k×8 bit low power consumption	70/85/100/120ns	113
CXK58257ATM CXK58257AYM				123
CXK58257AP -□□□□X CXK58257AM -□□□□X CXK58257ATM -□□□□X CXK58257AYM -□□□□X	256k bit	32k×8bit, Ta = -25 to 85°C TSOP is compatible with Mitsubishi type in the pin low power consumption	70/100/120ns	133
				143
CXK58257AP -12LB CXK58257AM -12LB CXK58257ATM -12LB CXK58257AYM -12LB	256k bit	32k×8bit, 3V operation possible TSOP is compatible with Mitsub- shi type in the pin low power consumption	120ns@4.5 to 5.5V 240ns@2.7 to 3.3V	153
				162
CXK58258AP CXK58258AJ	256k bit	32k×8bit	15*/20/25/35ns	171
CXK58258BP CXK58258BM CXK58258BJ	256k bit	32k×8bit low power consumption	20*/25/35ns	178
CXK58267AM CXK58267ATM CXK58267AYM	256k bit	32k×8bit, CE2 pin low power consumption	70/85/100/120ns	185
				196

* : under development

Type	Memorie capacity	Functions	Access time	Page
CXK59288P CXK59288J	288k bit	32k × 9bit	15*/17/20/25ns	207
CXK59289P CXK59289M*	288k bit	32k × 9bit	20/25ns	214
CXK59290M CXK59290TM	288k bit	32k × 9bit JEDEC standard	70/100/120ns	221
CXK581000P CXK581000M	1M bit	128k × 8bit	100/120/150ns	232
CXK581000P -□□□□ X CXK581000M -□□□□ X	1M bit	128k × 8bit Ta = -25 to 85°C	100/120/150ns	243
CXK581000P -12LB CXK581000M -12LB	1M bit	128k × 8bit, 3V operation possible	120ns@4.5 to 5.5V 240ns@2.7 to 3.3V	252
CXK581001P CXK581001M	1M bit	128k × 8bit	70/85ns	263
CXK581100TM CXK581100YM	1M bit	128k × 8bit	100/120/150ns	273
CXK581100TM -□□□□ X CXK581100YM -□□□□ X	1M bit	128k × 8 bit Ta = -25 to 85°C EIAJ standard	100/120/150ns	284
CXK581100TM -12LB CXK581100YM -12LB	1M bit	128k × 8bit, 3V operation possible EIAJ standard	120ns@4.5 to 5.5V 240ns@2.7 to 3.3V	293
CXK581020SP CXK581020J	1M bit	128k × 8bit	35/45/55ns	304
CXK581021J	1M bit	128k × 8bit	47ns	313
CXK581120J*	1M bit	128k × 8 bit	15/17/20ns	323
CXK584000TM* CXK584000YM* CXK584000M* CXK584000P*	4M bit	512k × 8bit Vcc = 2.7V to 5.5V low power consumption	55/70/85/100ns	330
CXK584001TM* CXK584001YM* CXK584001M* CXK584001P*	4M bit	512k × 8bit Vcc = 3V ± 10% low power consumption	100/120ns	340

* : under development

2) Apprication Specific Memories

Type	Application specific	Functions	Access time	Page
CXK7701J	Cache memorie	4k × 16bit × 2way	30/35/45ns	351
CXK77910J*		128k × 9bit Self Timed RAM	17/20ns	366

* : under development

3) Mask ROM

Type	Memorie capacity	Functions	Access time	Page
CXK384000	4M bit	256k × 16/512k × 8bit	200ns	377
CXK384001	4M bit	512k × 8bit	200ns	384
CXK388000	8M bit	512k × 16bit/1024k × 8bit	200ns	391

4) Nonvolatile Memories

• EEPROM

Type	Memory capacity	Functions	Page
CXK1023M CXK1023P	2048bit	256 × 8bit Serial I/O	401
CXK1024M CXK1024P	2048bit	128 × 16/256 × 8bit Serial I/O	409

• EPROM

Type	Memorie capacity	Functions	Access time	Page
CXK27C256DQ	256k bit	32k × 8bit	150/200ns	420
CXK27C512DQ	512k bit	64k × 8bit	150/200ns	430
CXK27C1000DQ	1M bit	128k × 8bit (1M Mask ROM pin compatible)	150/200ns	441
CXK27C1001DQ	1M bit	128K × 8bit (JEDEC standard)	150/200ns	451

Memorie Line-up

<h3>High Speed CMOS Static RAM</h3> <p>High Speed CMOS Static RAM series are the product of extensive research and experience in semiconductor manufacture accumulated over three decades of technical improvement. They represent the latest achievement in CMOS technology.</p> <p>In the quest for high reliability and easy use various ideal applications have been outlined.</p> <p>Features</p> <ul style="list-style-type: none"> ● High speed operation ● Low power consumption ● Complete static operation ● Input/Output TTL compatible ● Single supply operation 5V 	<p>SRAM</p> <ul style="list-style-type: none"> 64K BIT <ul style="list-style-type: none"> 8K x 8 <ul style="list-style-type: none"> CXK 5864B (70/100/120ns) CXK 5863 (25/30/35ns) CXK 5863A (20/25ns) CXK 5863B * (25/30/35ns) CXK 5866 * (15/20ns) CXK 5466 (15/20ns) CXK 5467 (15/20ns) 16K x 4 <ul style="list-style-type: none"> CXK 5971 (25/30/35ns) CXK 5971A * (25/30/35ns) CXK 5972 * (15/20ns) 72K BIT <ul style="list-style-type: none"> 8K x 9 <ul style="list-style-type: none"> CXK 58257A (70/85/100/120ns) CXK 58267A (70/85/100/120ns) CXK 58258A * (15/20/25ns) CXK 58258B * (20/25/35ns) 256K BIT <ul style="list-style-type: none"> 32K x 8 <ul style="list-style-type: none"> CXK 59290 * (70/100/120ns) CXK 59288 * (15/17/20/25ns) CXK 59288 * (20/25ns) 288K BIT <ul style="list-style-type: none"> 32K x 9 <ul style="list-style-type: none"> CXK 581000 (100/120/150ns) CXK 581100 (100/120/150ns) CXK 581001 (70/85ns) CXK 581020 (35/45/55ns) CXK 581021J * (47ns) CXK 581120J * (15/17/20ns) 1M BIT <ul style="list-style-type: none"> 128K x 8 <ul style="list-style-type: none"> CXK 584000 * (55/70/85/100ns) CXK 584001 * (100/120ns) 4M BIT <ul style="list-style-type: none"> 512K x 8 <ul style="list-style-type: none"> CXK 7701 (30/35/45ns) CXK 77910 * (17/20ns) <p>ASM</p> <ul style="list-style-type: none"> 128K BIT <ul style="list-style-type: none"> 8K x 16/4K x 16 x 2 <ul style="list-style-type: none"> CXK 7701 (30/35/45ns) 1M BIT <ul style="list-style-type: none"> 128K x 9 <ul style="list-style-type: none"> CXK 77910 * (17/20ns) <p>* Under development</p>
<h3>CMOS Mask ROM</h3> <p>CMOS Mask ROM series were bred from up to date CMOS technology. In terms of reliability and facility of usage they stand on their own.</p> <p>The very best has been accomplished to offer an exceptional range of applications for respective memories.</p> <p>Features</p> <ul style="list-style-type: none"> ● High speed operation ● Low power consumption ● Input/Output TTL compatible ● Single supply operation 5V ● Short time delivery 	<p>MASK ROM</p> <ul style="list-style-type: none"> 4M BIT <ul style="list-style-type: none"> 512K x 8 <ul style="list-style-type: none"> CXK 384001 (200ns) 256K x 16 <ul style="list-style-type: none"> CXK 384000 (200ns) 8M BIT <ul style="list-style-type: none"> 512K x 16 <ul style="list-style-type: none"> CXK 388000 (200ns)

EEPROM Non-volatile Memorie	<p>EEPROM non-volatile memory series are PROM element provided the ability of electrically erase and program, written data do not get erased even if the supply voltage is cut.</p> <p>Features</p> <ul style="list-style-type: none"> ● Memory retention time with no power supply Over 10 years ● Erase/Write times Over 10^5 times ● One word unit rewrite possible ● CMOS (CXK1024P) ● High speed operation ($f=1\text{MHz}$, CXK1024P/M) 	
CMOS EPROM	<p>CMOS EPROM series are PROM devices that permit electrical writing and erasing through ultra violet radiation. The adoption of CMOS in the peripheral circuits realizes high speed operation and low power consumption. The series are most suitable for large capacity program memories.</p> <p>Features</p> <ul style="list-style-type: none"> ● High speed operation ● Low current consumption ● I/O TTL compatible ● Output 3-state output ● High speed program mode ● 5V single supply operation for reading 	

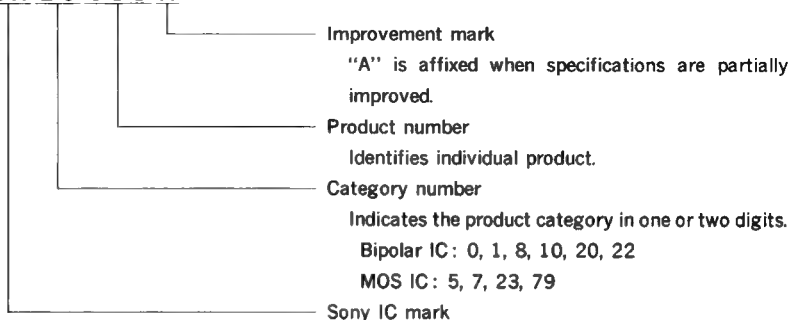
3. IC Nomenclature

1) Nomenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

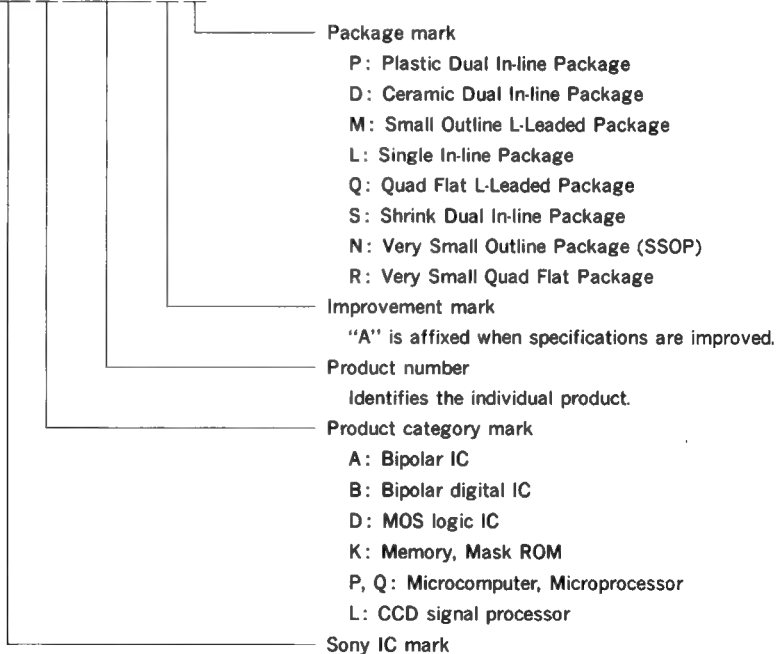
(1) Conventional nomenclature system

[Example] C X 2 0 0 1 1 A



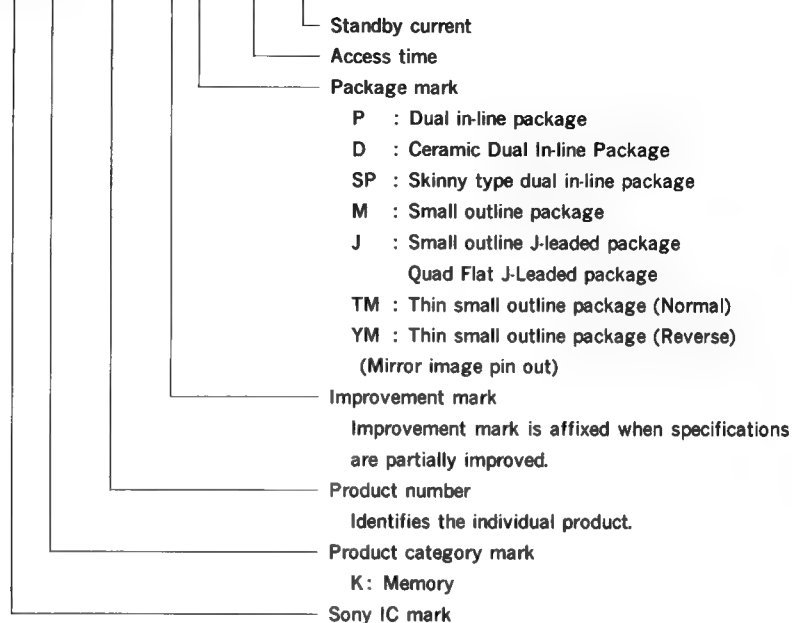
(2) New nomenclature

[Example] C X A 1 0 0 1 A P



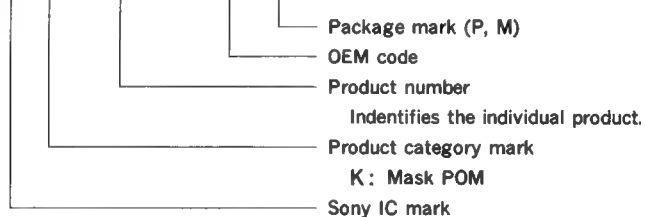
(3) Memory nomenclature

[Example] C X K 5 4 6 4 A P — □ □ □ □



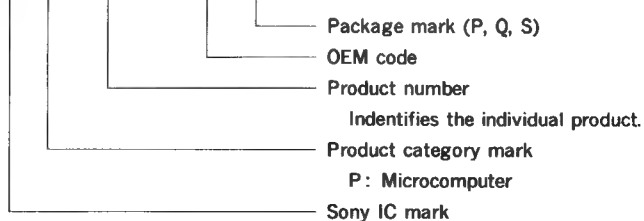
(4) Mask ROM nomenclature

[Example] C X K 3 8 1 2 8 — □ □ □ □



(5) Microcomputer nomenclature

[Example] C X P 5 0 6 8 — □ □ □ □



4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even for a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably shortened.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage V_{CC} (V_{DD})

The maximum voltage that can be applied between the power supply pin and ground pin.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit. The transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation P_D

The maximum power consumption allowed in IC.

Usage beyond the Allowable power dissipation will cause ultimate destruction through the IC's heat generation.

(3) Operating ambient temperature T_{opr}

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at $T_a = 25^\circ\text{C}$ are not guaranteed even in this temperature range.

(4) Storage temperature T_{stg}

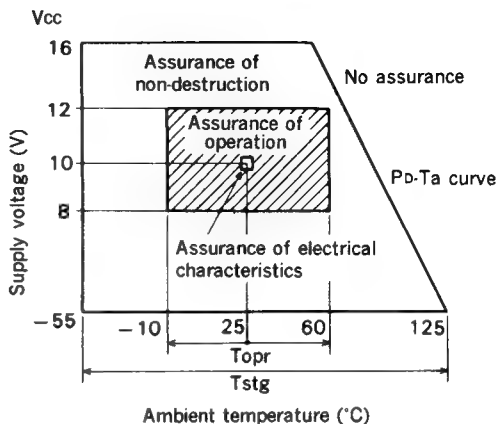
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage V_{in} , output voltage V_{out} , input current I_{in} , output current I_{out} and other values may be specified in some IC's.

A general example on the relation with Absolute Maximum Ratings.



Main points on Circuit design.

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following :

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with amount of IC integration in package types.

2) Protection against electrostatic breakdown

There have been problems concerning electrostatic destruction of electronic devices since the 2nd World War. Those are closely related to the advancement made in the field of semiconductor devices; this is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

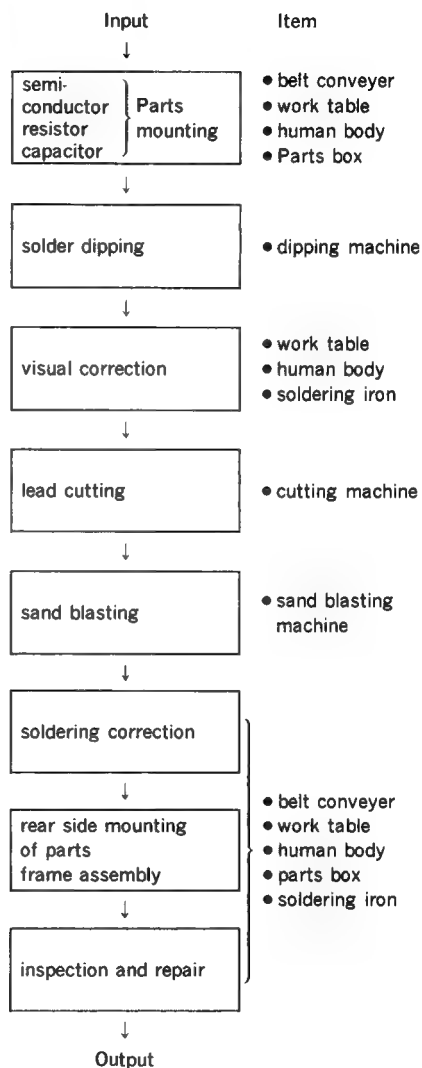
Electrostatic destruction is again drawing people's attention as we are entering the era of LSI, VLSI, and ULSI. Here are our suggestions for preventing such destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below :

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for the prevention of electrostatic destruction

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

- ① Equalize potentials of terminals when transporting or storing.
- ② Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.
- ③ Prepare an environment that does not generate static electricity.

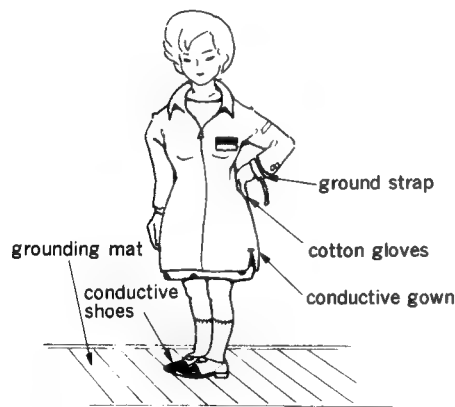
One method is keeping relative humidity in the work room to about 50%.

Operator

(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

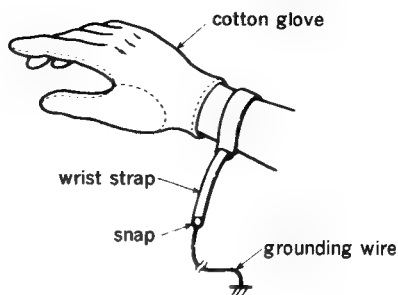
protective clothing for static electricity



(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm.

example of grounding band

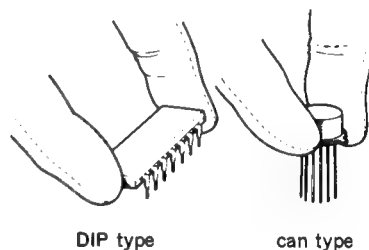


When using a copper wire for grounding, connect a $1\text{M}\Omega$ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



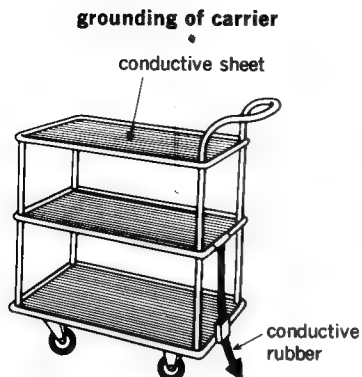
Equipment and tools

(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

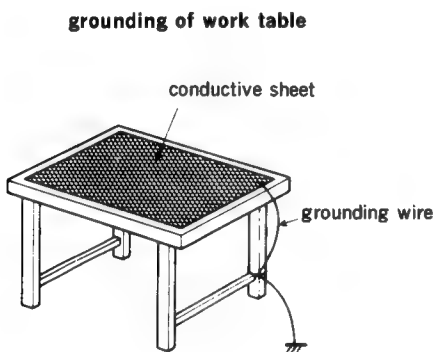
[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks



(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.



(3) Semiconductor device case

Use a conductive case.

(4) Insertion of semiconductor device

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet.

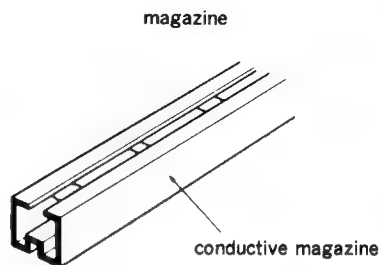
(5) Other points of caution

Take note of the kind of brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

Transporting, storing and packaging methods

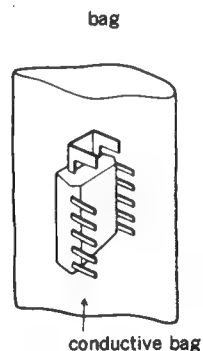
(1) Magazine

Use conductive, or antistatic-treated plastic IC magazines.



(2) Bag

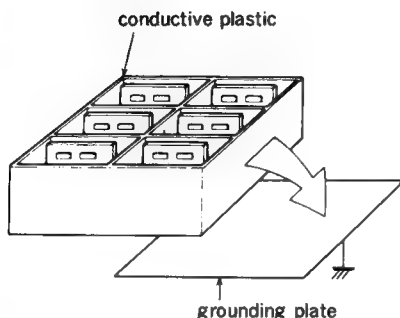
Use a conductive bag to store ICs.



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of conductive plastic. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



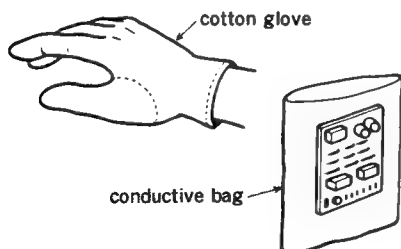
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table for discharging.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive bag. Do not use a polyethylene bag.

handling of mounted substrate

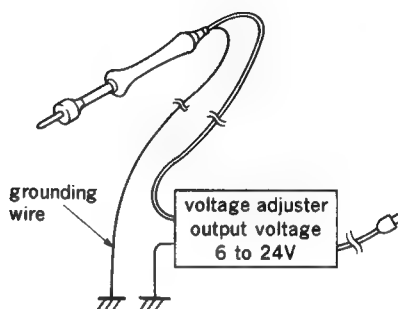


Soldering operation

(1) Soldering iron

Use a soldering iron with a grounding wire and an insulation resistance greater than $10M\Omega$ (DC 500V) after five minutes from energizing.

example of solder iron tip grounding



(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves.

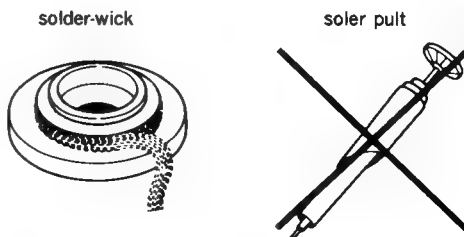
(4) Manual soldering

Solder with wrist strap connected to the hand.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.

solder remover



3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2".

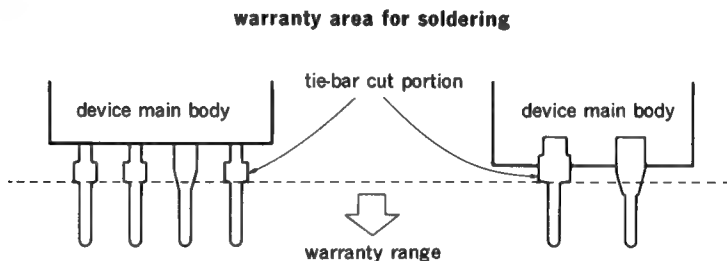
An abstract of this standard follows:

- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which been heated to $230^{\circ}\text{C} \pm 5^{\circ}\text{C}$ for 5 ± 1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10 ± 1 seconds in a solder bath of $260^{\circ}\text{C} \pm 5^{\circ}\text{C}$, or for 3 ± 0.5 seconds in a solder bath of $350^{\circ}\text{C} \pm 10^{\circ}\text{C}$, for a distance of up to 1 to 1.5 mm from the main body.

For the solder flow system temperature should be $260^{\circ}\text{C} \pm 5^{\circ}\text{C}$. To solder by soldering iron temperature should be $350^{\circ}\text{C} \pm 10^{\circ}\text{C}$.

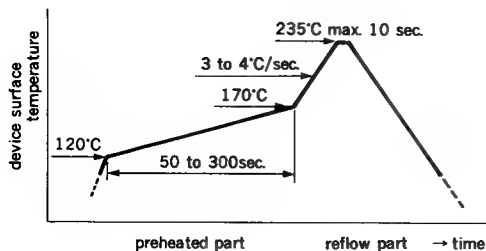
- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at $260^{\circ}\text{C} \pm 5^{\circ}\text{C}$. The distance between the device main body and solder bath is 1.6 mm.

(2) Resistance to soldering heat when mounting infrared reflow.

When surface mount devices (SOP, QFP etc) are dipped directly into a solder pot, the device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



5. Quality Assurance and Reliability

The Concept to Quality Assurance

There are 2 fundamental principles guiding Sony Semiconductors.

1. Customer satisfaction
2. Top level performance

What comes first is the ability to respond convincingly to given requirements in terms of Quality, Delivery, Cost and Servicing. This involves all operations involved in the process. The second requisite is the quest for superior accomplishment. Here, talent is demanded to fulfill customer expectations, where quality is concerned, and pursue related activities.

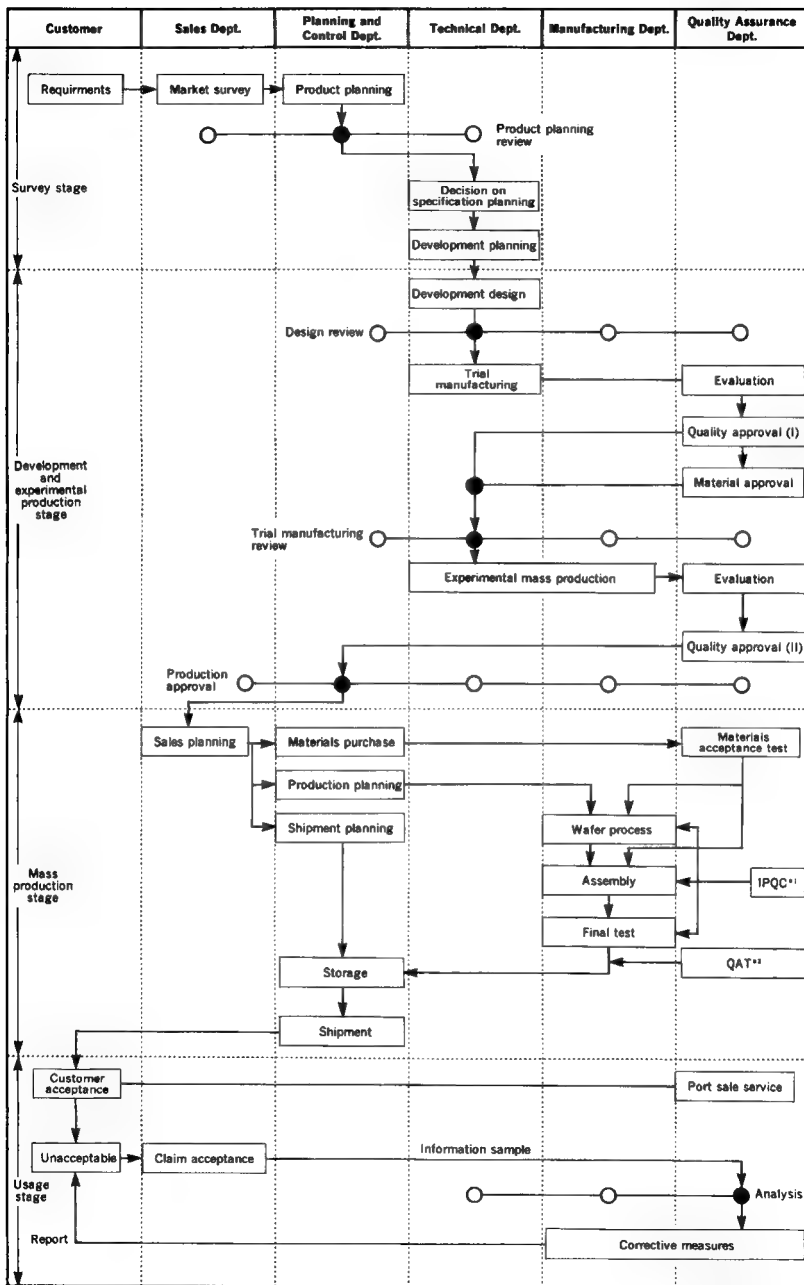
To this effect an elaborate system of quality assurance is firmly established. From the early stages of research and development well into production, sales and servicing,

orderly control is applied for the maintenance of high standards and further improvement. Systematization and automation are pushed ahead to provide a stable output of high quality production.

In this respect, the force in charge of implementing the program is nonetheless subject to constant polishing. Gifted people well aware of the problems inherent to their tasks are at the core of the excellence reflected on their yield.

With the aim of providing the most economical, the most useful and at the same time the most gratifying products where quality is the criterion, Sony keeps fueling a relentless urge for achievement.

Quality assurance system of semiconductor products



*1. IPQC: In Process Quality Control
 *2. QAT: Quality Assurance Test

Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-

inspected" at the final fabrication stage, thus ensuring no defective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodic Reliability Test

Item		Testing time	LTPD
Electrical Characteristics Test		In order to know the initial quality level, some types are selected and tested again.	
Life Test	high temperature operation	up to 1000 h	10%
	high temperature and high humidity with bias	up to 1000 h	10%
	pressure cooker	up to 200 h	10%
Environmental Test	soldering heat resistance	10s	15%
	heat cycle	100 cycles	15%
Mechanical Test	solderability	Japan Industrial	15%
	length strength	Standard (JIS)	15%
Other Tests		If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.	

*These tests are selected by sampling standard.

LTPD: Lot Tolerance Percent Defective

These tests and inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

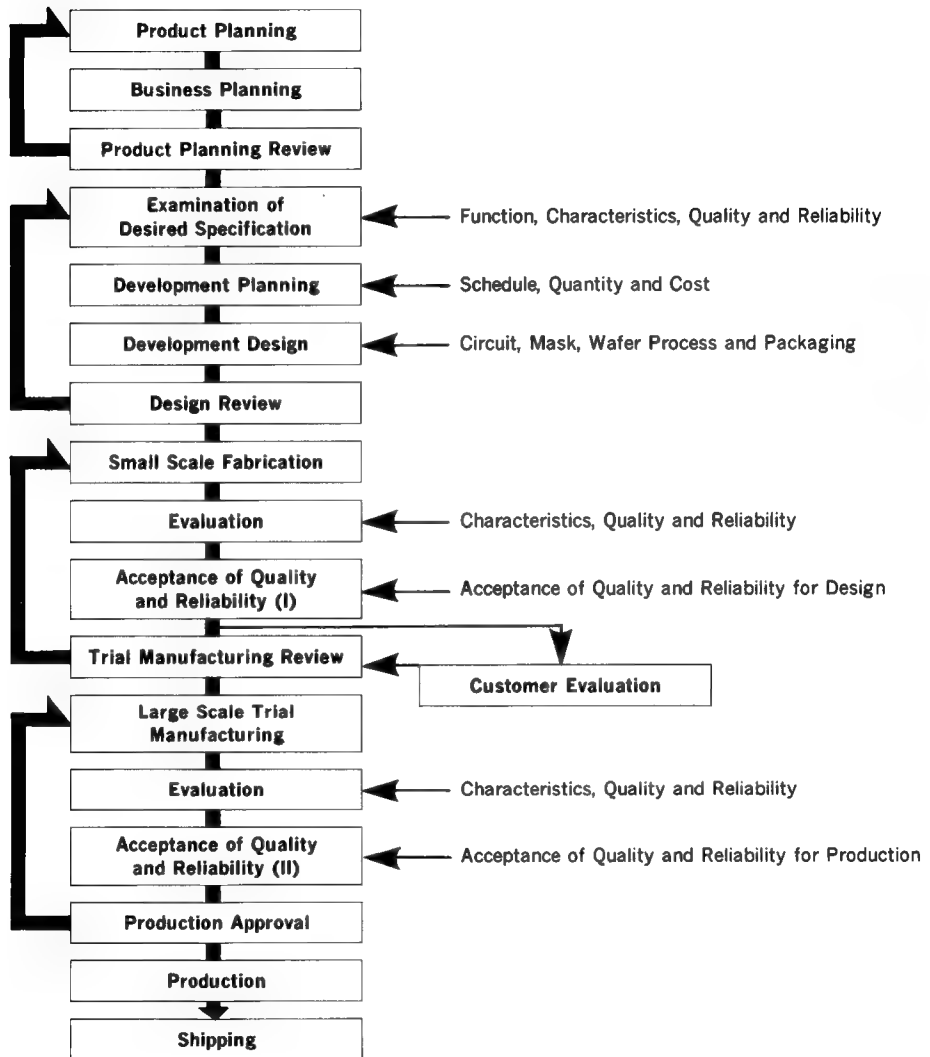
Reliability Test Standards

Types of test	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C	Typical	1000h	5%
High temperature storage	Ta=150°C		1000h	5%
Low temperature storage	Ta= -65°C		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH	Typical	1000h	5%
Pressure cooker	Ta=121°C 100%RH 203kPa		96h	5%
Temperature cycle	Ta= -65°C to +150°C		100c	10%
Heat shock	Ta= -65°C to +150°C		100c	10%
Soldering heat resistance	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 15,000m/s ² Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 200m/s ² 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 200,000m/s ² Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)	based on JIS			10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

LTPD: Lot Tolerance Percent Defective

Flow Chart from Development to Manufacturing

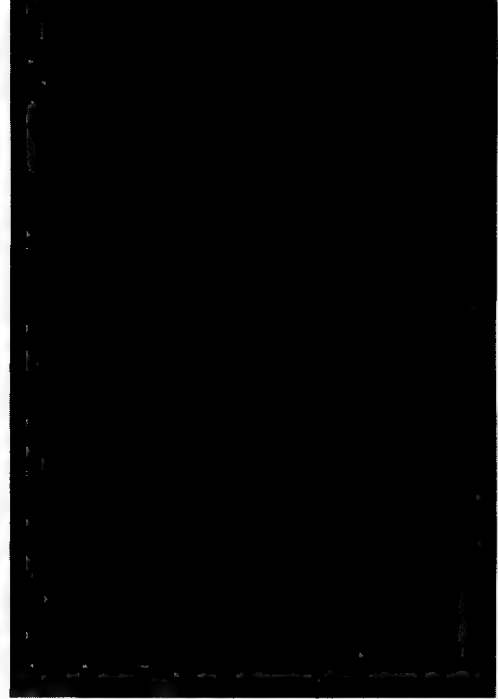
Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.



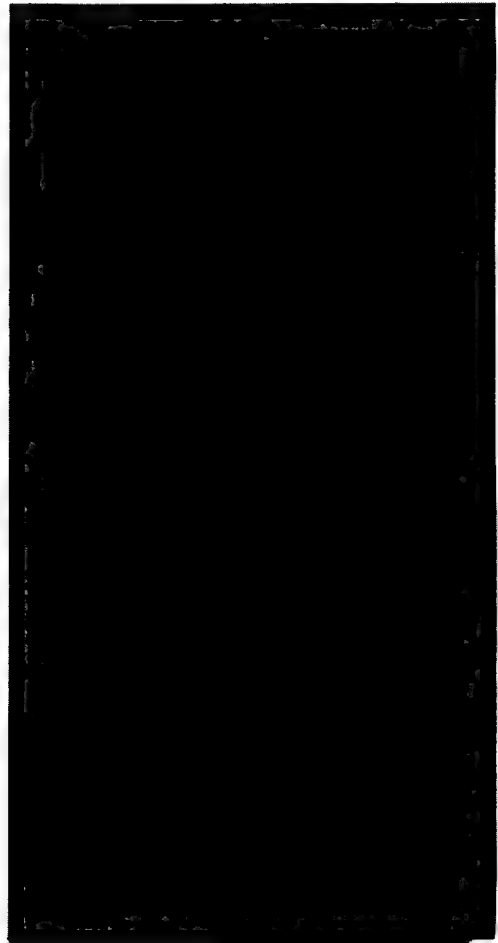
Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	D I P	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		S I P	SINGLE IN-LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		Z I P	ZIG-ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		P G A	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
	Surface mounted	Standard flat package	Q F P	QUAD FLAT L-LEADED PACKAGE	P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
			S O P	SMALL OUTLINE L-LEADED PACKAGE	P	1.27mm (50MIL)	Gull-Wing	2-direction
		Standard 2-direction chip carrier	S O J	SMALL OUTLINE J-LEADED PACKAGE	P	1.27mm (50MIL)	J-Lead	2-direction
		Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE	P	0.5mm	Gull-Wing	4-direction
			VSOP	VERY SMALL OUTLINE PACKAGE	P	0.65mm	Gull-Wing	2-direction
			TSOP	THIN SMALL OUTLINE PACKAGE	P	0.5mm (0.55mm)	Gull-Wing	2-direction
		Standard chip carrier	Q F J	QUAD FLAT J-LEADED PACKAGE	P	1.27mm (50MIL)	J-Lead	4-direction
			Q F N	QUAD FLAT NON-LEADED PACKAGE	C	1.27mm (50MIL)	Leadless	Package under side

* P.....Plastic, C.....Ceramic



Static RAM



1) Static RAM

Type	Memorie capacity	Functions	Access time	Page
CXK5864BP CXK5864BSP CXK5864BM	64k bit	8k×8bit	70/100/120ns	30
CXK5863P CXK5863M CXK5863J	64k bit	8k×8bit	25/30/35ns	40
CXK5863AP CXK5863AJ	64k bit	8k×8bit	20/25/30ns	50
CXK5863BP CXK5863BJ CXK5863BM	64k bit	8k×8bit	25/30/35ns	57
CXK5866P CXK5866J	64k bit	8k×8bit	15/20ns	65
CXK5466P CXK5466J	64k bit	16k×4bit	15/20ns	72
CXK5467P CXK5467J	64k bit	16k×4bit, \overline{OE} pin	15/20ns	80
CXK5971AP CXK5971AM CXK5971AJ	72k bit	8k×9bit	25/30/35ns	88
CXK5971P CXK5971M CXK5971J	72k bit	8k×9bit	25/30/35ns	96
CXK5972P CXK5972J	72k bit	8k×9bit	15/20ns	106
CXK58257AP CXK58257ASP CXK58257AM	256k bit	32k×8 bit low power consumption	70/85/100/120ns	113
CXK58257ATM CXK58257AYM				123
CXK58257AP □□□□ X CXK58257AM □□□□ X	256k bit	32k×8bit, Ta= -25 to 85°C TSOP is compatible with Mitsubishi type in the pin low power consumption	70/100/120ns	133
CXK58257ATM □□□□ X CXK58257AYM □□□□ X				143
CXK58257AP -12LB CXK58257AM -12LB	256k bit	32k×8bit, 3V operation possible TSOP is compatible with Mitsubi- shi type in the pin low power consumption	120ns@4.5 to 5.5V 240ns@2.7 to 3.3V	153
CXK58257ATM -12LB CXK58257AYM -12LB				162
CXK58258AP CXK58258AJ	256k bit	32k×8bit	15*/20/25/35ns	171
CXK58258BP CXK58258BM CXK58258BJ	256k bit	32k×8bit low power consumption	20*/25/35ns	178
CXK58267AM	256k bit	32k×8bit, CE2 pin low power consumption	70/85/100/120ns	185
CXK58267ATM CXK58267AYM				196

* : under development

Type	Memorie capacity	Functions	Access time	Page
CXK59288P CXK59288J	288k bit	32k×9bit	15*/17/20/25ns	207
CXK59289P CXK59289M*	288k bit	32k×9bit	20/25ns	214
CXK59290M CXK59290TM	288k bit	32k×9bit JEDEC standard	70/100/120ns	221
CXK581000P CXK581000M	1M bit	128k×8bit	100/120/150ns	232
CXK581000P -□□□□ X CXK581000M -□□□□ X	1M bit	128k×8bit Ta = -25 to 85°C	100/120/150ns	243
CXK581000P -12LB CXK581000M -12LB	1M bit	128k×8bit, 3V operation possible	120ns@4.5 to 5.5V 240ns@2.7 to 3.3V	252
CXK581001P CXK581001M	1M bit	128k×8bit	70/85ns	263
CXK581100TM CXK581100YM	1M bit	128k×8bit	100/120/150ns	273
CXK581100TM -□□□□ X CXK581100YM -□□□□ X	1M bit	128k×8 bit Ta = -25 to 85°C EIAJ standard	100/120/150ns	284
CXK581100TM -12LB CXK581100YM -12LB	1M bit	128k×8bit, 3V operation possible EIAJ standard	120ns@4.5 to 5.5V 240ns@2.7 to 3.3V	293
CXK581020SP CXK581020J	1M bit	128k×8bit	35/45/55ns	304
CXK581021J	1M bit	128k×8bit	47ns	313
CXK581120J*	1M bit	128k×8 bit	15/17/20ns	323
CXK584000TM* CXK584000YM* CXK584000M* CXK584000P*	4M bit	512k×8bit Vcc=2.7V to 5.5V low power consumption	55/70/85/100ns	330
CXK584001TM* CXK584001YM* CXK584001M* CXK584001P*	4M bit	512k×8bit Vcc=3V±10% low power consumption	100/120ns	340

* : under development

SONY**CXK5864BP/BSP/BM** -70L/10L/12L/
-70LL/10LL/12LL**8,192-word × 8-bit High Speed CMOS Static RAM****Description**

CXK5864BP/BSP/BM are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8 bits and operates from a single 5V supply. These IC are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time (Access time)
CXK5864BP/BSP/BM-70L, 70LL 70ns(Max.)
CXK5864BP/BSP/BM-10L, 10LL 100ns(Max.)
CXK5864BP/BSP/BM-12L, 12LL 120ns(Max.)
- Low power operation :
CXK5864BP/BSP/BM-70LL, 10LL, 12LL ;
Standby/Operation : 5 μ W (Typ.) / 40mW (Typ.)
CXK5864BP/BSP/BM-70L, 10L, 12L ;
Standby/Operation : 10 μ W (Typ.) / 40mW (Typ.)
- Single power supply 5V : $+5V \pm 10\%$
- Fully static memory ... No clock or timing strobe required
- Equal access and cycle time
- Common data input and output : three state output
- Directly TTL compatible : All inputs and outputs
- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

CXK5864BP
28 pin DIP (Plastic)



CXK5864BSP
28 pin DIP (Plastic)



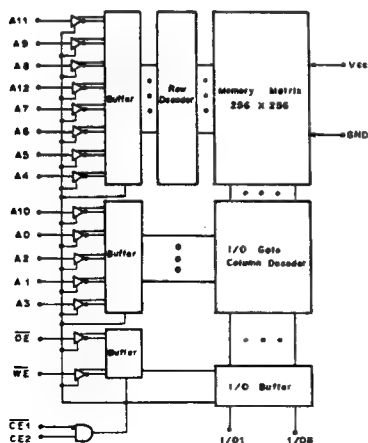
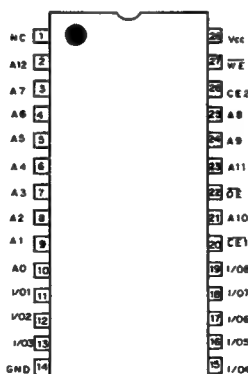
CXK5864BM
28 pin SOP (Plastic)

**Function**

8,192-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration
(Top View)****Pin Description**

Symbol	Description
A0 to A7	Address input
I/O0 to I/O7	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK5864BP/BSP	1.0
		CXK5864BM	0.7
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

● DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	- 70L/10L/12L - 70LL/10LL/12LL			Unit
			Min.	Typ.*	Max.	
Input leak current	I _{LI}	V _{IN} = GND to V _{CC}	-500	—	500	nA
Output leak current	I _{LO}	V _{I/O} = GND to V _{CC} CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL}	-500	—	500	nA
Operating supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	8	15	mA
Average operating current	I _{CC2}	Min. cycle Duty = 100%, I _{OUT} = 0mA	—	30	50	mA
Standby current	I _{SB1}	CE2 ≤ 0.2V	- L	—	2	μA
		or { CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V	- LL	—	1	
	I _{SB2}	CE1 = V _{IH} or CE2 = V _{IL}	—	0.1	2	mA
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C

Pin capacitance

(T_a = 25°C, f = 1MHz)

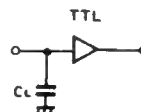
Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Input/Output capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item		Conditions
Input pulse high level		V _{IH} = 2.2V
Input pulse low level		V _{IL} = 0.8V
Input rise time		t _r = 5ns
Input fall time		t _f = 5ns
Input and output reference level		1.5V
Output load conditions	10L/10LL/12L/12LL	C _L * = 100pF, 1TTL
	70L/70LL	C _L * = 30pF, 1TTL

* C_L includes scope and jig capacitances.

● Read cycle

Item	Symbol	- 70L/70LL		- 10L/10LL		- 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	100	—	120	ns
Chip enable access time ($\overline{\text{CE1}}$, CE2)	t _{CO1} t _{CO2}	—	70	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	50	—	60	ns
Output hold from address change	t _{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} t _{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z (OE)	t _{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} * t _{HZ2} *	0	30	0	35	0	45	ns
Output disable to output in high Z (OE)	t _{OHZ} *	0	30	0	35	0	45	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

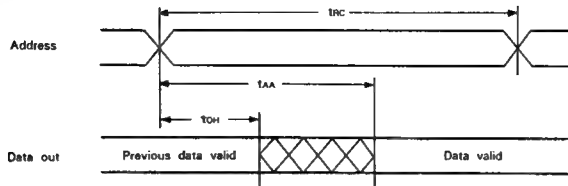
● Write cycle

Item	Symbol	- 70L/70LL		- 10L/10LL		- 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	60	—	80	—	85	—	ns
Chip enable to end of write	t _{CW}	60	—	80	—	85	—	ns
Data to write time overlap	t _{DW}	30	—	35	—	50	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	40	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{CE1}}$, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	30	0	35	0	45	ns

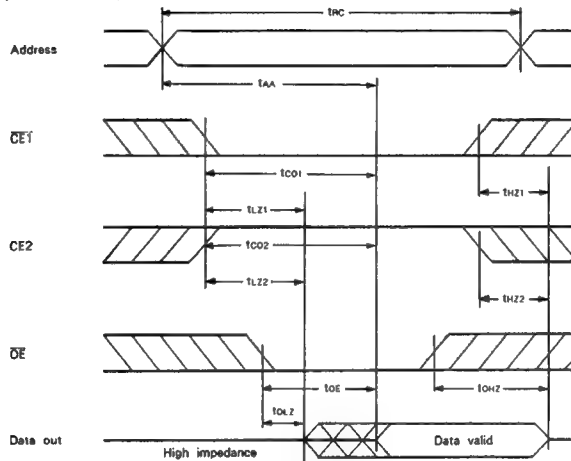
* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

Timing Waveform

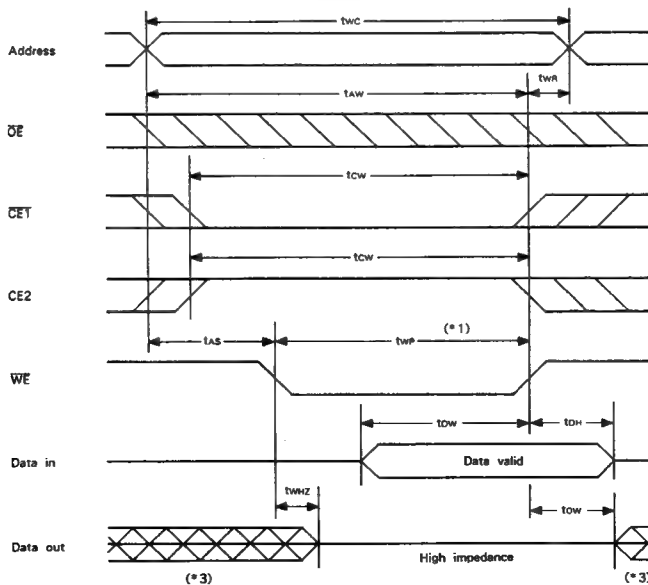
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



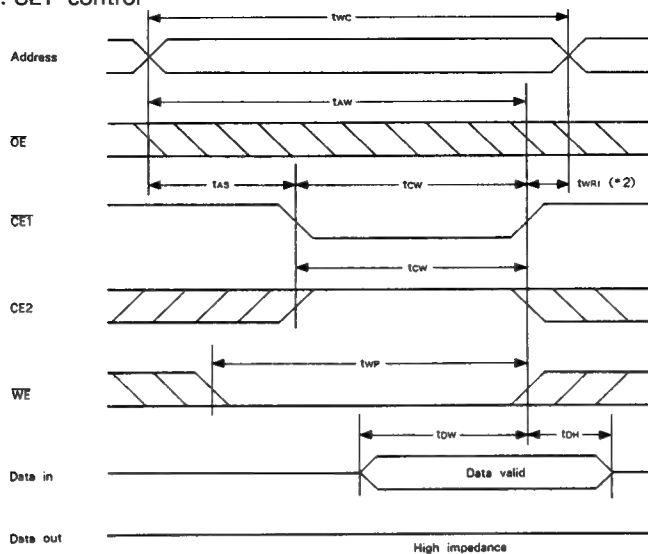
- Read cycle (2) : $\overline{WE} = V_{IH}$



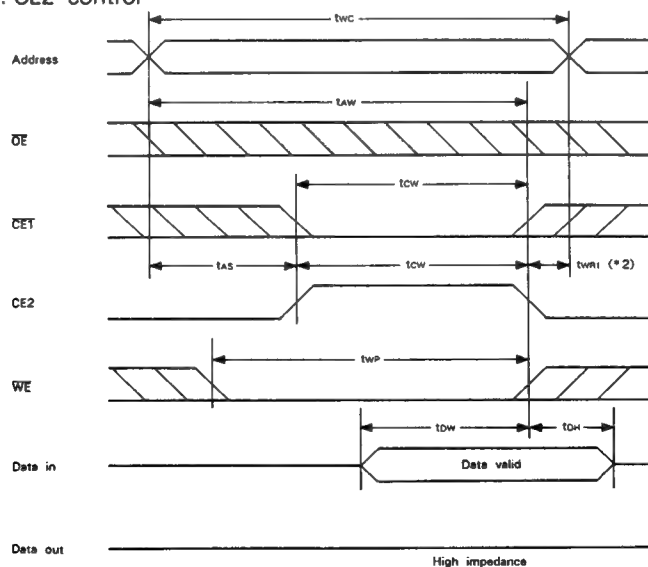
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



Note)

- *1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- *2. t_{WR1} is tested from either the rising edge of $\overline{\text{CE1}}$ or the falling edge of CE2 , whichever comes earlier, until the end of the write cycle.
- *3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

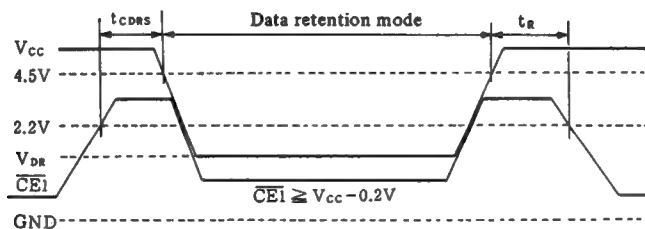
Data Retention Characteristics

(Ta = 0 to +70°C)

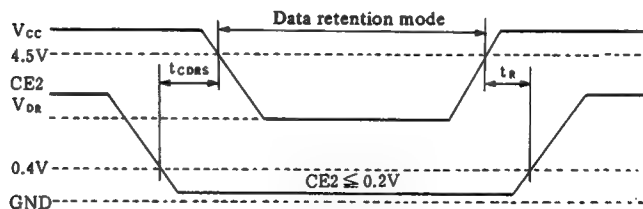
Item	Symbol	Test conditions		- 70L/10L/12L			- 70LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	*1	Ta = 0°C to 70°C	—	1	35	—	0.5	15	μA
		V _{CC} = 3.0V	Ta = 0°C to 40°C	—	—	—	—	—	3	
	I _{CCDR2}	V _{CC} = 2.0 to 5.5V, *1		—	2	60	—	1	30	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t _R			t _{RC} *2	—	—	t _{RC} *2	—	—	ns

* 1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ [$\overline{CE1}$ Control] or $CE2 \leq 0.2V$ [$CE2$ Control]* 2. t_{RC}: Read cycle time

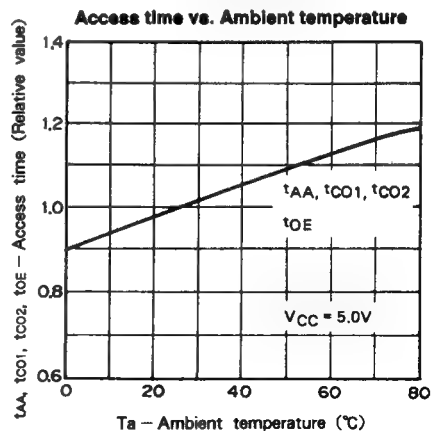
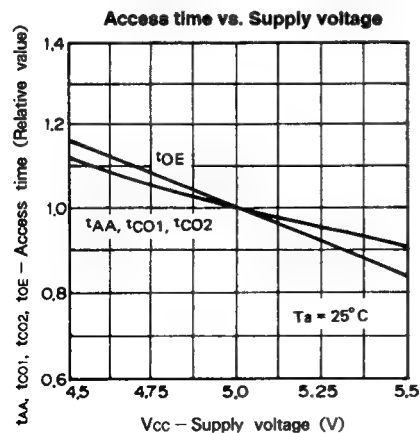
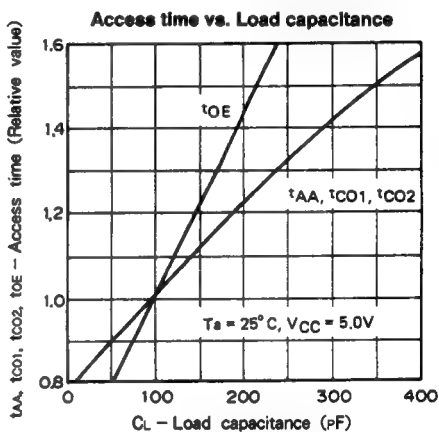
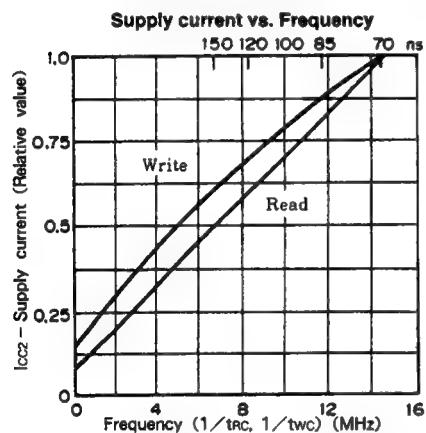
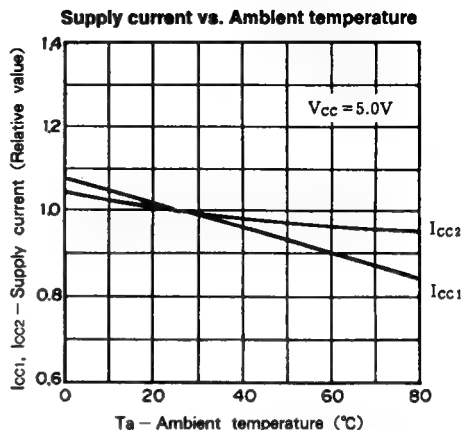
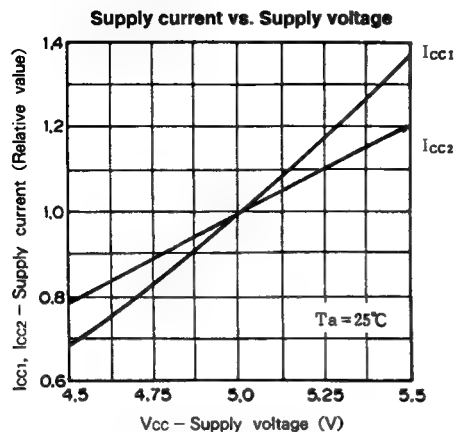
Data Retention Waveform

1. $\overline{CE1}$ control

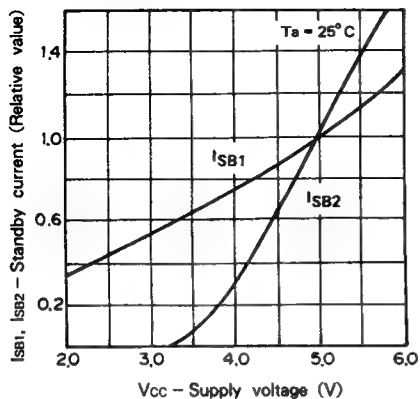
2. CE2 control



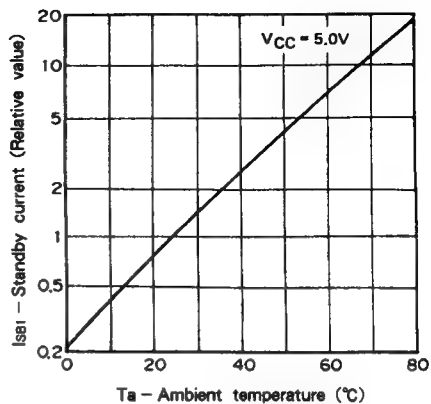
Example of Representative Characteristics



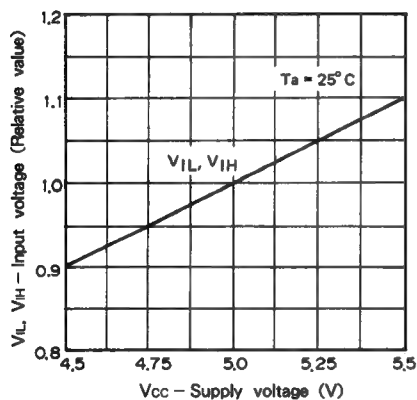
Standby current vs. Supply voltage



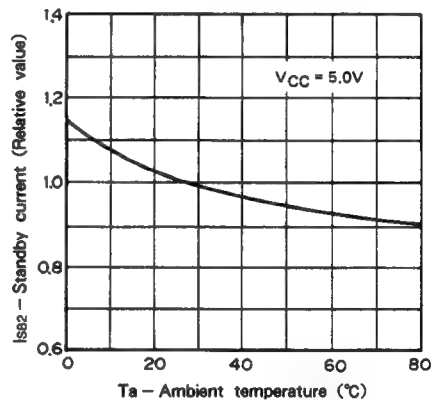
Standby current vs. Ambient temperature



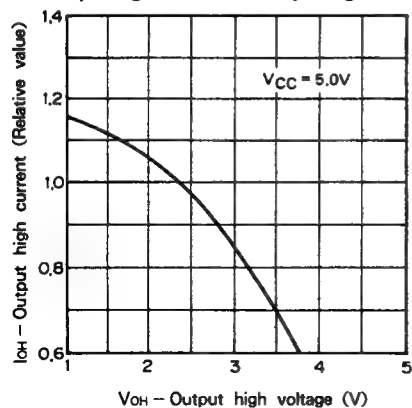
Input voltage level vs. Supply voltage



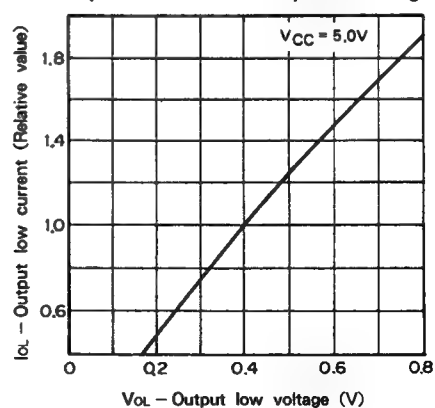
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



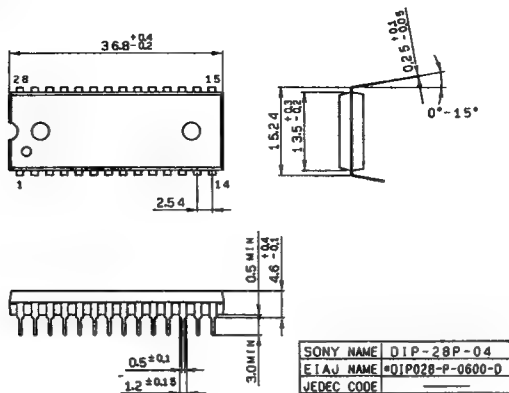
Output low current vs. Output low voltage



Package Outline Unit : mm

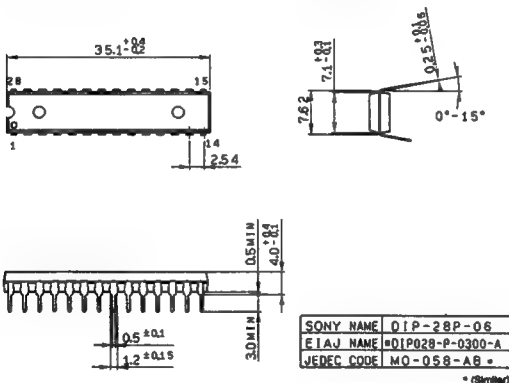
CXK5864BP

28 pin DIP (Plastic) 600mil 4.2g



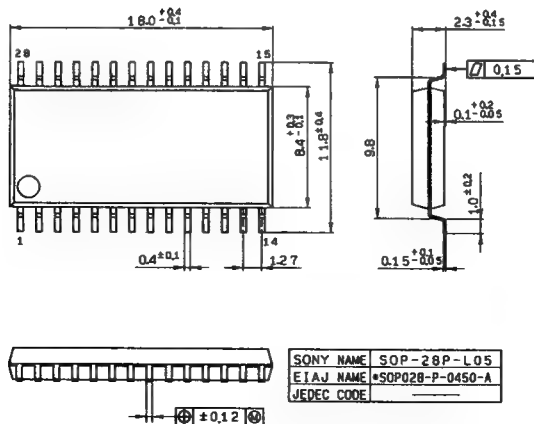
CXK5864BSP

28 pin DIP (Plastic) 300mil 2.0g



CXK5864BM

28 pin SOP (Plastic) 450mil 0.7g



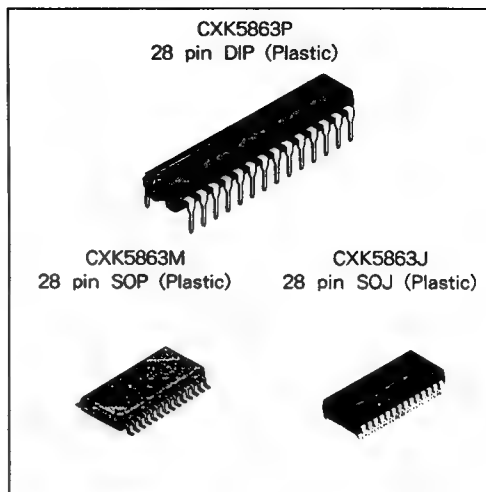
8192-word \times 8-bit High Speed CMOS Static RAM

Description

CXK5863P/M/J are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8-bit and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time 25ns/30ns/35ns (Max.)
- Low power standby 5 μ W (Typ.)
- Low power operation 150mW (Typ.)
- Single + 5V supply : 5V \pm 10 %
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Low voltage data retention 2.0V (Min.)
- Full CMOS.
- Available in 28 pin 300mil DIP, 450mil SOP, 300mil SOJ.



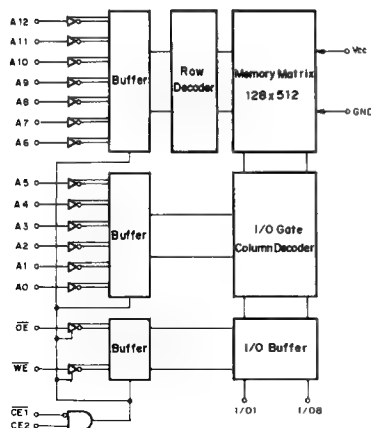
Structure

Silicon gate CMOS IC

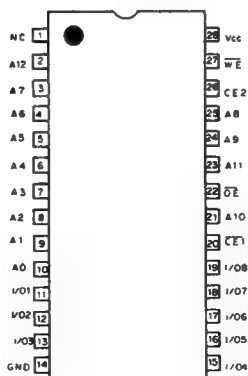
Function

8192-word \times 8-bit static
RAM

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
$\overline{CE}1$, CE2	Chip enable 1, 2 input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
V _{cc}	+ 5V Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

Ta = 25°C, GND = 0V

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK5863P/J	1.0
		CXK5863M	0.7
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature	T _{solder}	260 ± 10	°C · sec

*Note) V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

Ta = 0 to + 70°C, GND = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

*Note) V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

 $V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0$ to $+70^\circ C$

Item	Symbol	Test condition	- 25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	$V_{IN} = GND$ to V_{CC}	-1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O} = GND$ to V_{CC} , $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OUT} = 0mA$	—	30	60	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, $I_{OUT} = 0mA$	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	1	100	μA
	I_{SB2}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH}	—	10	25	mA
Output high voltage	V_{OH}	$I_{OH} = -4.0mA$	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0mA$	—	—	0.4	V

* $V_{CC} = 5V$, $T_a = 25^\circ C$

I/O capacitance

 $T_a = 25^\circ C$, $f = 1MHz$

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF

Note) This parameter is sampled and is not 100% tested.

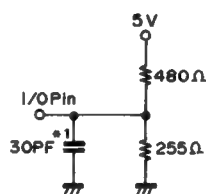
AC characteristics

● AC test conditions

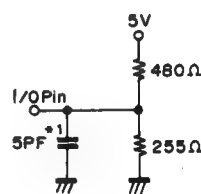
 $V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ C$

Item	Condition
Input pulse high level	$V_{IH} = 3.0V$
Input pulse low level	$V_{IL} = 0V$
Input rise time	$t_r = 5ns$
Input fall time	$t_f = 5ns$
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* 1. including scope and jig capacitance

* 2. for t_{LZ1} , t_{LZ2} , t_{OLZ} , t_{HZ1} , t_{HZ2} , t_{OHZ} , t_{OW} , t_{WHZ}

Fig. 1

• Read cycle

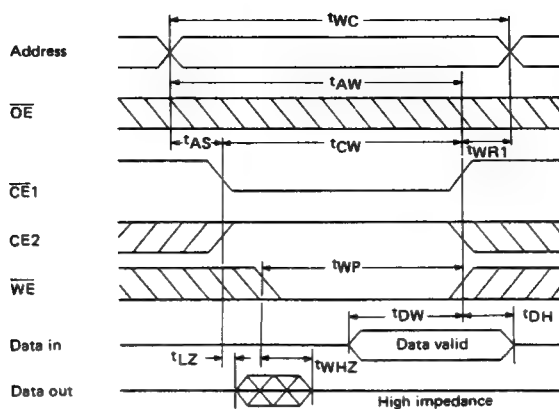
Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time (CE1)	t _{CO1}	—	25	—	30	—	35	ns
Chip enable access time (CE2)	t _{CO2}	—	25	—	30	—	35	ns
Output enable to output valid	t _{OE}	—	15	—	15	—	20	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} * t _{LZ2} *	5	—	5	—	5	—	ns
Output enable to output in low Z (OE)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} * t _{HZ2} *	0	15	0	15	0	20	ns
Chip disable to output in high Z (OE)	t _{OHZ} *	0	13	0	13	0	15	ns
Chip enable to power up time (CE1, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time (CE1, CE2)	t _{PD}	—	20	—	20	—	20	ns

• Write cycle

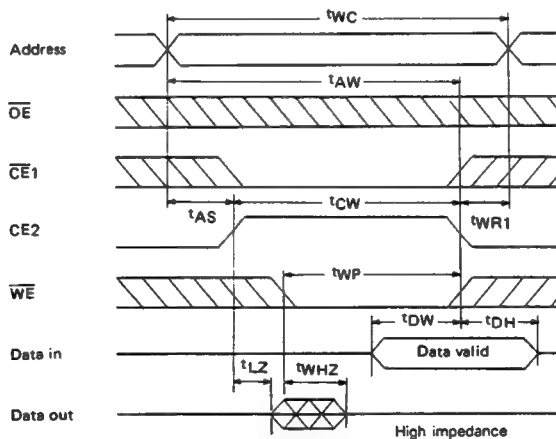
Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	20	—	20	—	30	—	ns
Chip enable to end of write	t _{CW}	20	—	20	—	30	—	ns
Data to write time overlap	t _{DW}	12	—	12	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	20	—	20	—	25	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	13	0	13	0	15	ns

* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

• Write cycle No. 2 : [$\overline{\text{CE1}}$ control]



• Write cycle No. 3 : [CE2 control]

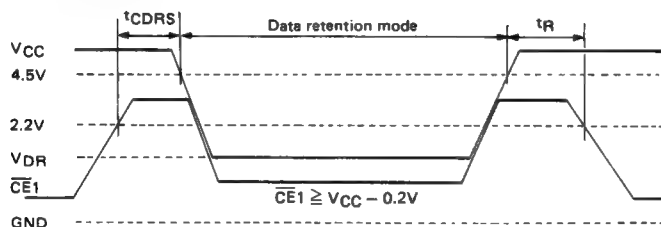
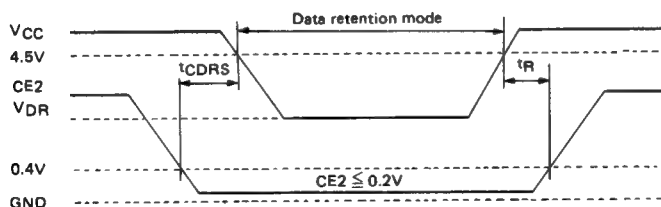


During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

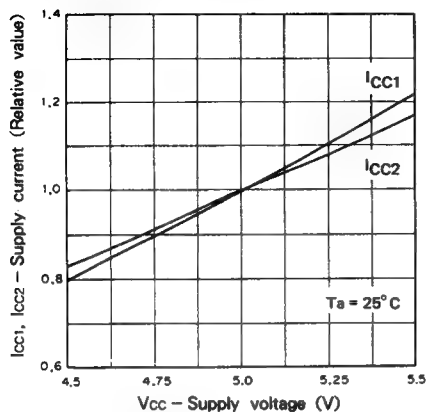
 $T_a = 0 \text{ to } +70^\circ\text{C}$

Item	Symbol	Test condition	-25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0\text{V} \text{ *1}$	—	0.5	50	μA
	I_{CCDR2}	$V_{CC} = 2.0 \text{ to } 5.5\text{V} \text{ *1}$	—	1.0	100	μA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		$t_{RC} \text{ *2}$	—	—	ns

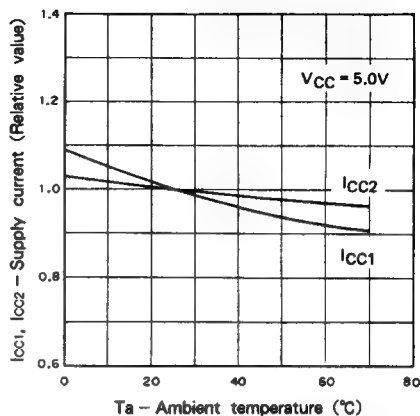
*1 $\overline{CE1} \geq V_{CC} - 0.2\text{V}$ or $CE2 \leq 0.2\text{V}$, $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$ *2 t_{RC} : Read cycle timeData Retention Waveform (1) : [$\overline{CE1}$ control]Data Retention Waveform (2) : [$CE2$ control]

Example of Representative Characteristics

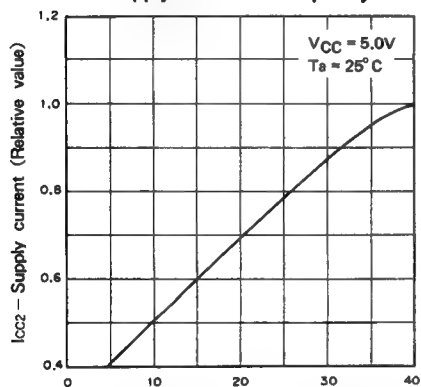
Supply current vs. Supply voltage



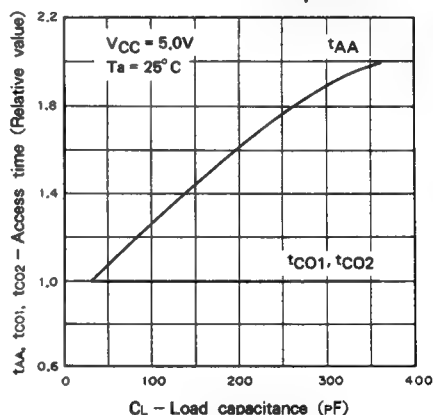
Supply current vs. Ambient temperature



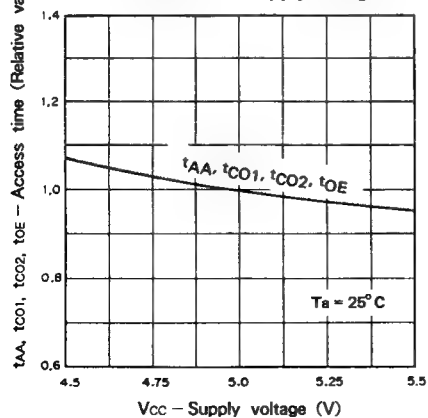
Supply current vs. Frequency



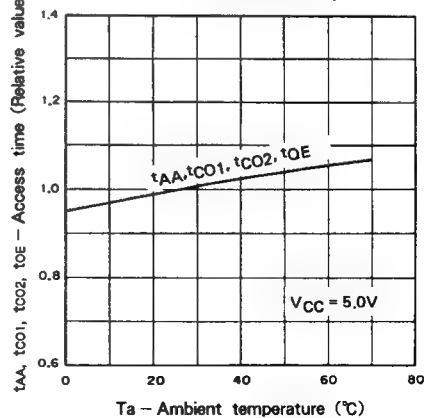
Access time vs. Load capacitance



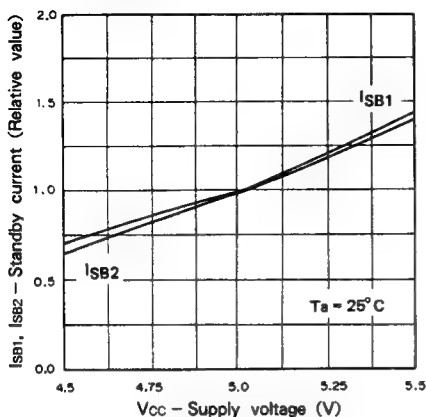
Access time vs. Supply voltage



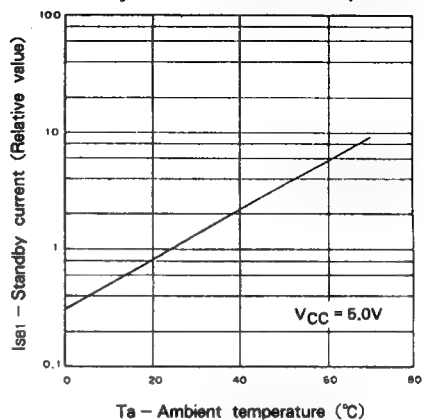
Access time vs. Ambient temperature



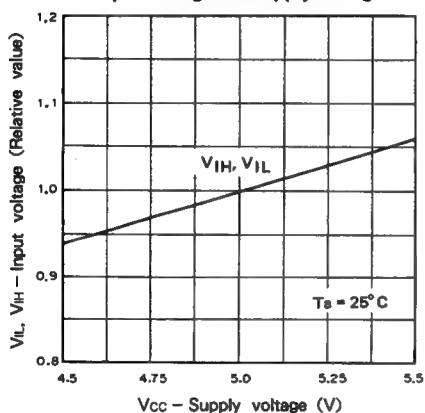
Standby current vs. Supply voltage



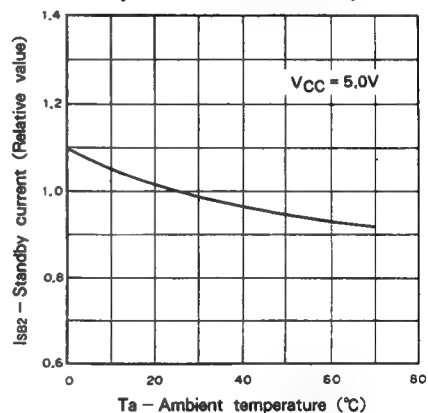
Standby current vs. Ambient temperature



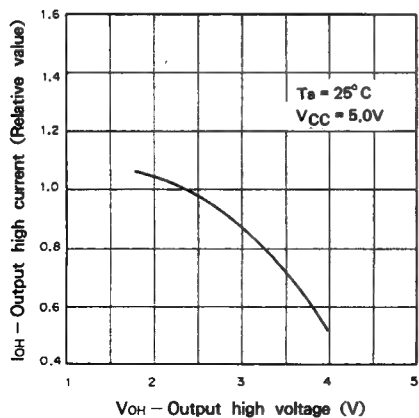
Input voltage vs. Supply voltage



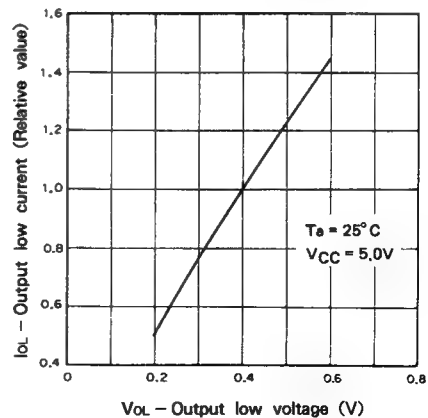
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



CXK5863P 28 pin DIP (Plastic) 300mil 2.0g



The drawing shows the mechanical specifications for the SOP-28P-L05 package. It includes three views: a top view, a side view, and an end view.

- Top View:** Shows a rectangular package with 28 pins. The overall width is $18.0^{+0.4}_{-0.1}$ mm. The pin pitch is $0.4^{+0.1}_{-0.1}$ mm. The distance from the center of the package to the center of the pins is $8.4^{+0.3}_{-0.1}$ mm. The distance from the center of the package to the center of the pins on the opposite side is $11.8^{+0.4}_{-0.1}$ mm. The distance from the center of the package to the center of the pins on the same side is 1.27 mm. The distance from the center of the package to the center of the pins on the opposite side is 1.4 mm. The distance from the center of the package to the center of the pins on the same side is 1.27 mm. The distance from the center of the package to the center of the pins on the opposite side is 1.4 mm.
- Side View:** Shows the package height. The overall height is 9.8 mm. The distance from the top of the package to the top of the pins is $2.3^{+0.4}_{-0.15}$ mm. The distance from the top of the package to the top of the pins is 0.15 mm. The distance from the top of the package to the top of the pins is $0.1^{+0.2}_{-0.05}$ mm. The distance from the top of the package to the top of the pins is $1.0^{+0.2}_{-0.1}$ mm. The distance from the top of the package to the top of the pins is $0.15^{+0.05}_{-0.05}$ mm.
- End View:** Shows the package width. The overall width is $0.4^{+0.1}_{-0.1}$ mm. The distance from the center of the package to the center of the pins is 1.27 mm. The distance from the center of the package to the center of the pins is 1.4 mm. The distance from the center of the package to the center of the pins is 1.27 mm. The distance from the center of the package to the center of the pins is 1.4 mm.

Technical drawing of the SOJ-28P-01 connector, showing dimensions in millimeters.

Top View Dimensions:

- Overall Width: 18.42 ± 0.12
- Overall Height: 8.51 ± 0.12
- Pin Pitch: 2.54
- Pin Width: 1.5
- Central Cutout Width: 7.62 ± 0.12
- Distance from Left Edge to Hole: 0.73 ± 0.08
- Distance from Right Edge to Pin: 1.27

Side View Dimensions:

- Height: 0.2 ± 0.01
- Pin Diameter: 0.22 ± 0.02

Detail View Dimensions:

- Pin Diameter: 0.43 ± 0.1
- Pin Length: 0.95
- Hole Diameter: $\varnothing 0.17 \pm 0.01$

Scale: 0.1

Part Number: SOJ-28P-01

8192 word × 8-bit High Speed CMOS Static RAM
Description

CXK5863AP/AJ are 65,536 bits high speed CMOS static RAMS organized as 8,192 words by 8-bits and operate from a single 5V supply. These devices are suitable for use in high speed applications such as cash memory.

Features

- Fast access time : 20ns/25ns/30ns (Max.)
- Low power operation : 250mW (Typ.)
- Single + 5V supply : $5V \pm 10\%$
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Full CMOS.
- Compatible with various types of packages
CXK5863AP 300mil 28pin DIP package
CXK5863AJ 300mil 28pin SOJ package

CXK5863AP
28 pin DIP (Plastic)



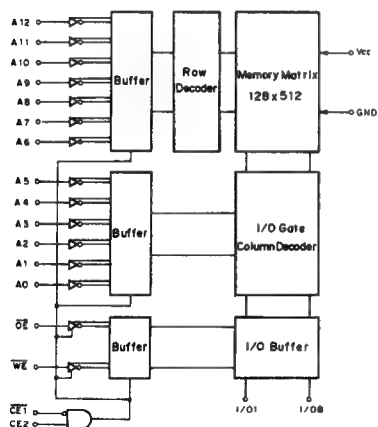
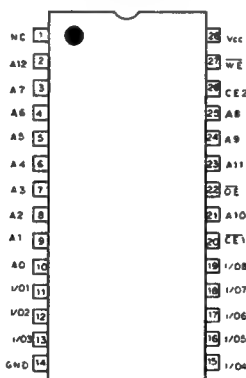
CXK5863AJ
28 pin SOJ (Plastic)


Structure

Silicon gate CMOS IC

Function

8192 word × 8-bit static RAM

Block Diagram

**Pin Configuration
(Top View)**

Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test condition	- 20			- 25/- 30			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	- 1	—	1	- 1	—	- 1	μA
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL}	- 1	—	1	- 1	—	1	μA
Operating power supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	50	80	—	50	80	mA
Average operating current	I _{CC2}	Cycle = Min, Duty = 100%, I _{OUT} = 0mA	—	95	130	—	70	90	mA
Standby current	I _{SB1}	CE1 ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	1	—	—	1	mA
	I _{SB2}	CE1 = V _{IH} or CE2 = V _{IL} , V _{IN} = V _{IL} or V _{IH}	—	10	25	—	10	25	mA
Output high voltage	V _{OH}	I _{OH} = - 4.0mA	2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

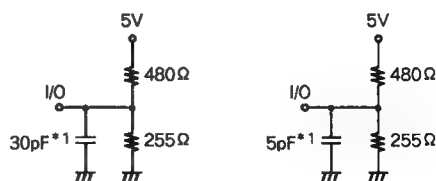
AC characteristics

● AC test conditions

(V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1) Output Load (2) *2



*1 including scope and jig capacitance

*2 for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

1) Read cycle

Item	Symbol	- 20		- 25		- 30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	20	—	25	—	30	—	ns
Address access time	t _{AA}	—	20	—	25	—	30	ns
Chip enable access time (CE1)	t _{CO1}	—	20	—	25	—	30	ns
Chip enable access time (CE2)	t _{CO2}	—	20	—	25	—	30	ns
Output enable to output valid	t _{OE}	—	10	—	12	—	12	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LEZ1} *, t _{LEZ2} *	5	—	5	—	5	—	ns
Output enable to output in low Z (OE)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	0	10	0	12	0	12	ns
Chip disable to output in high Z (OE)	t _{OHZ} *	0	8	0	10	0	10	ns
Chip enable to power up time (CE1, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time (CE1, CE2)	t _{PD}	—	20	—	20	—	20	ns

2) Write cycle

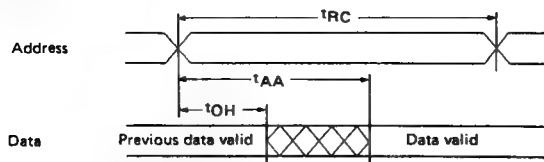
Item	Symbol	- 20		- 25		- 30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	20	—	25	—	30	—	ns
Address valid to end of write	t _{AW}	15	—	20	—	20	—	ns
Chip enable to end of write	t _{CW}	15	—	20	—	20	—	ns
Data to write time overlap	t _{DW}	10	—	12	—	12	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	15	—	20	—	20	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	10	0	12	0	12	ns

* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

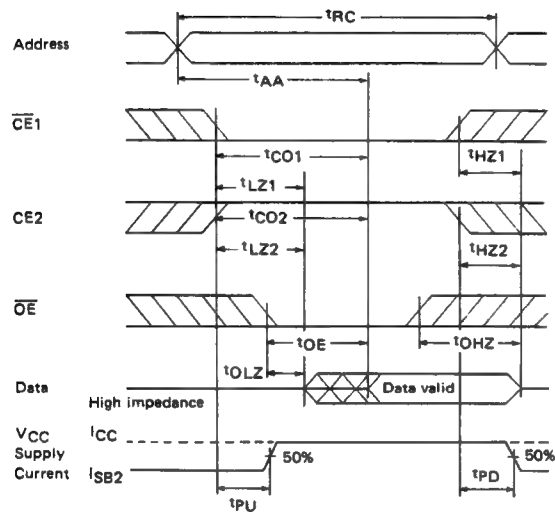
Timing Waveform

1) Read cycle

- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$

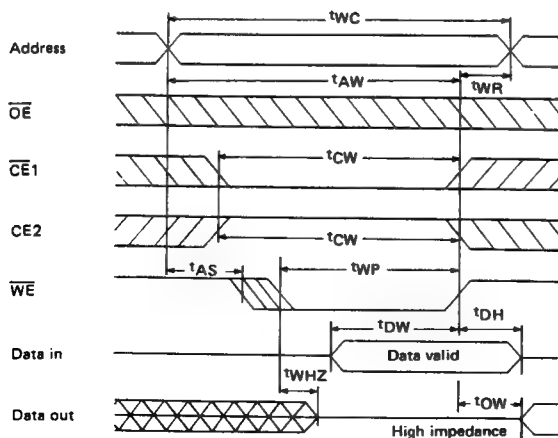


- Read cycle (2) : $\overline{WE} = V_{IH}$

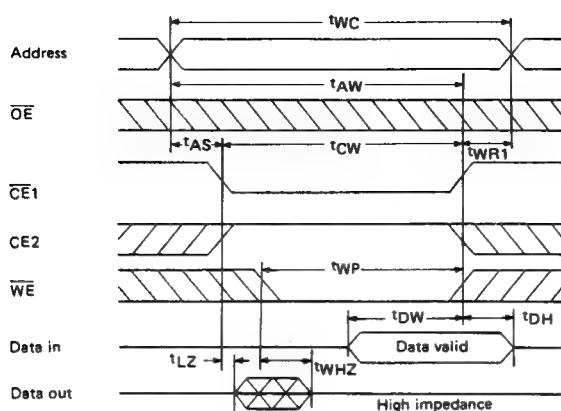


2) Write cycle

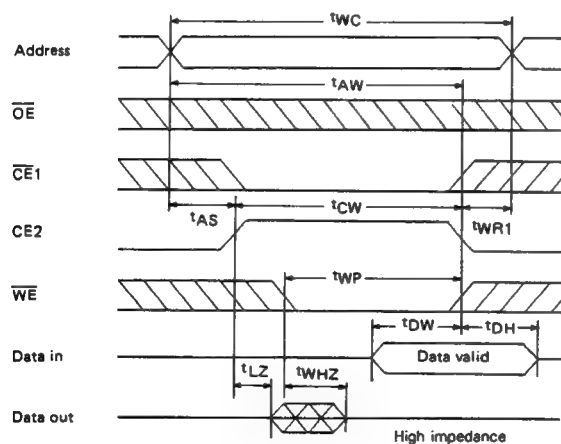
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE1}}$ control



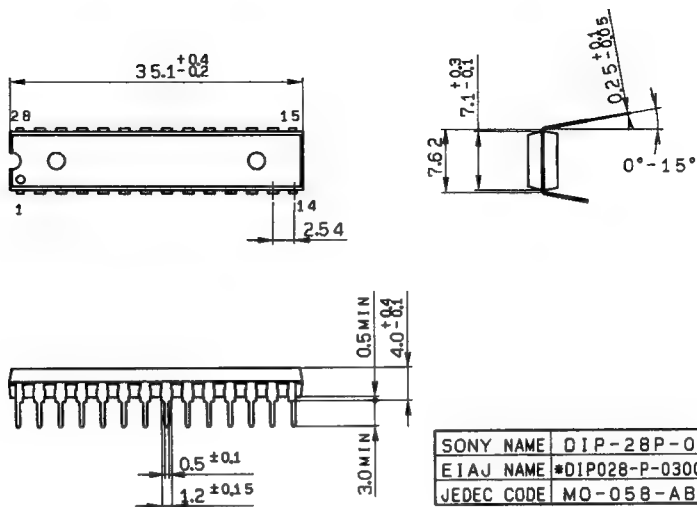
• Write cycle (3) : CE2 control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

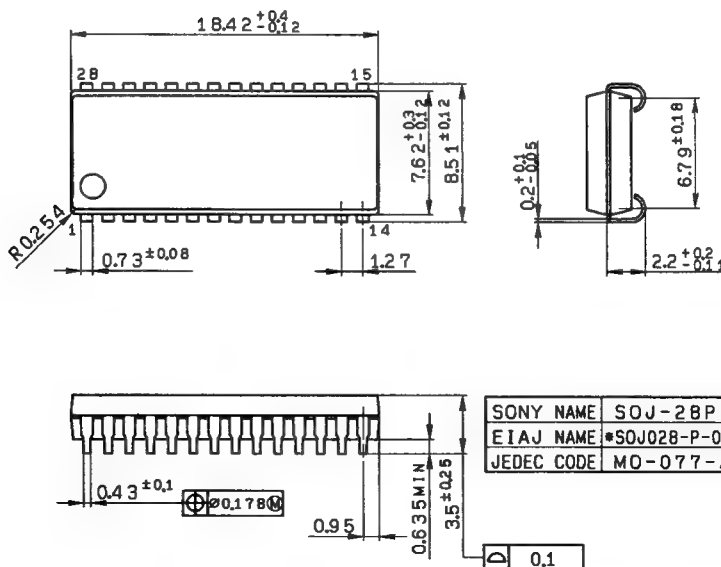
Package Outline Unit : mm

CXK5863AP 28pin DIP (Plastic) 300mil 2.0g



*(Similar)

CXK5863AJ 28pin SOJ (Plastic) 300mil 0.8g



SONY® CXK5863BP/BM/BJ-25/30/35

8192-word × 8-bit High Speed CMOS Static RAM

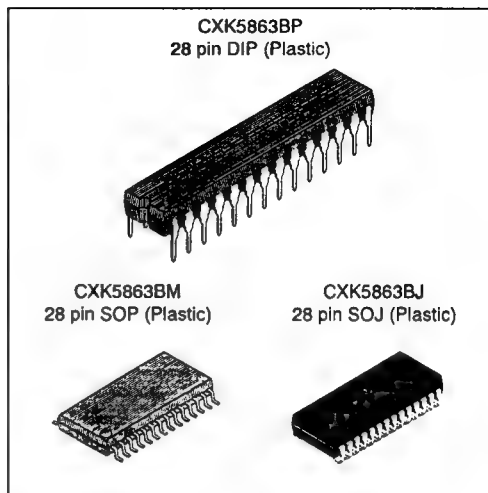
Preliminary

Description

CXK5863BP/BM/BJ are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8-bit and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time 25ns/30ns/35ns (Max.)
- Low power standby 5 μ W (Typ.)
- Low power operation 300mW (Typ., Cycle=Min.)
- Single + 5V supply: 5V \pm 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three state output.
- Directly TTL compatible: all inputs and outputs.
- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin 300mil DIP, 450mil SOP, 300mil SOJ.



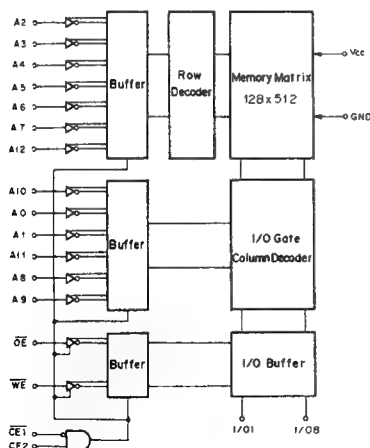
Function

8192-word × 8-bit static RAM

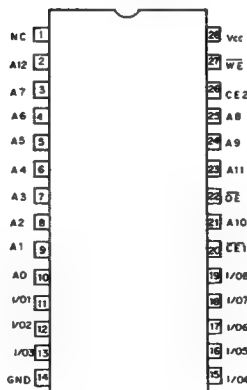
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 * to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK5863BP/BJ	1.0
		CXK5863BM	0.7
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature	T _{solder}	260 ± 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O}=-3.5V Min. for pulse width less than 20ns.**Truth Table**

$\overline{CE1}$	CE2	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL}=-3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test condition	- 25/30/35			Unit
			Min.	Typ. *	Max.	
Input leakage current	I _{II}	V _{IN} =GND to V _{CC}	-1	—	1	μA
Output leakage current	I _{LO}	V _{IO} =GND to V _{CC} , $\overline{CE1}=V_{IH}$ or $CE2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$	-1	—	1	μA
Operating power supply current	I _{CC1}	$\overline{CE1}=V_{IL}$, $CE2=V_{IH}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	—	—	—	mA
Average operating current	I _{CC2}	Cycle=Min, Duty=100%, I _{OUT} =0mA	—	60	90	mA
Standby current	I _{SB1}	$\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$ V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	—	1	100	μA
	I _{SB2}	$\overline{CE1}=V_{IH}$ or $CE2=V_{IL}$, V _{IN} =V _{IH} /V _{IL} , Cycle=Min.	—	10	25	mA
Output high voltage	V _{OH}	I _{OH} =-4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =8.0mA	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O Capacitance

(T_a=25 °C, f=1MHz)

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{IO} =0V	—	6	pF

Note) This parameter is sampled and is not 100% tested.

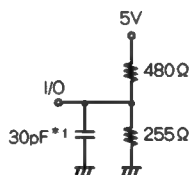
AC Characteristics

● AC test conditions

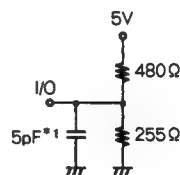
(V_{CC}=5V ± 10%, T_a=0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} =3.0V
Input pulse low level	V _{IL} =0V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2) *2



* 1. including scope and jig capacitance

* 2. for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WH2}

Fig. 1

• Read cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{\text{CE1}}$)	t _{CO1}	—	25	—	30	—	35	ns
Chip enable access time (CE2)	t _{CO2}	—	25	—	30	—	35	ns
Output enable to output valid	t _{OE}	—	12	—	12	—	15	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{\text{CE1}}$, CE2)	t _{LZ1} * t _{LZ2} *	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{\text{CE1}}$, CE2)	t _{HZ1} * t _{HZ2} *	0	12	0	12	0	15	ns
Chip disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	0	10	0	10	0	12	ns
Chip enable to power up time ($\overline{\text{CE1}}$, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time ($\overline{\text{CE1}}$, CE2)	t _{PD}	—	20	—	20	—	20	ns

• Write cycle

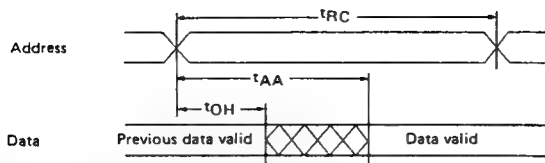
Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	20	—	20	—	30	—	ns
Chip enable to end of write	t _{CW}	20	—	20	—	30	—	ns
Data to write time overlap	t _{DW}	12	—	12	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	20	—	20	—	25	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{CE1}}$, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	12	0	12	0	15	ns

* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

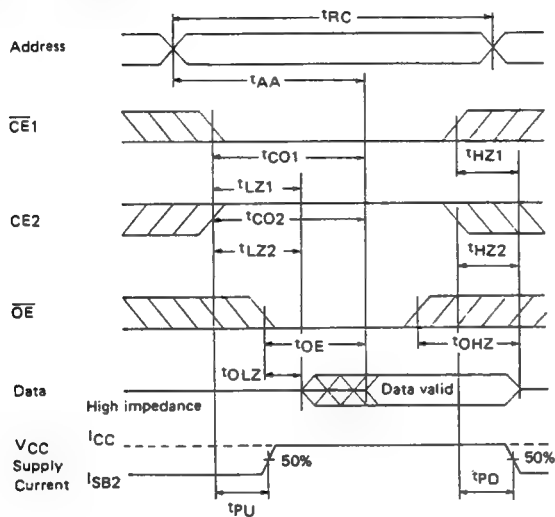
This parameter is sampled and is not 100% tested.

Timing Waveform

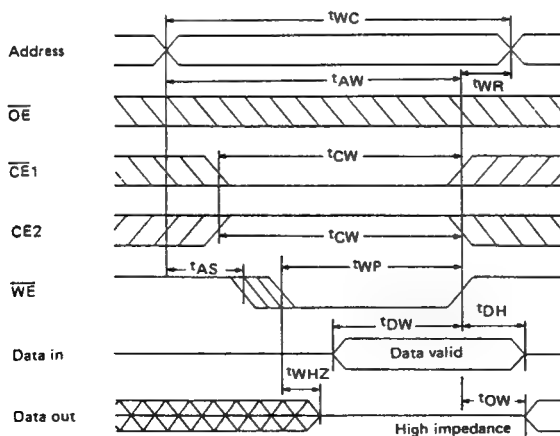
- Read cycle (1): $\overline{CE1}=\overline{OE}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



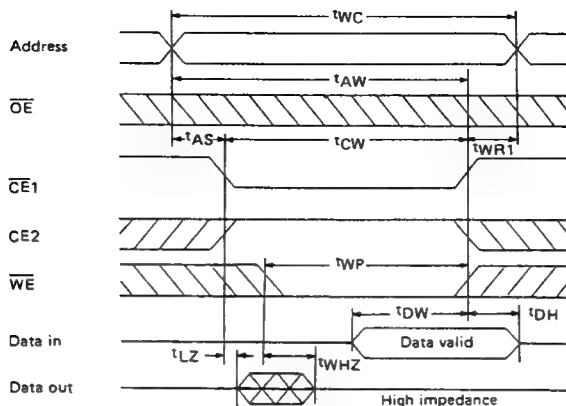
- Read cycle (2): $\overline{WE}=V_{IH}$



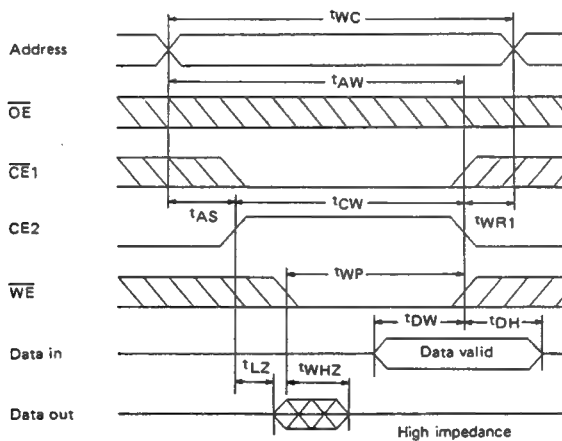
- Write cycle (1): \overline{WE} control



• Write cycle (2): $\overline{CE1}$ control



• Write cycle (3): $CE2$ control

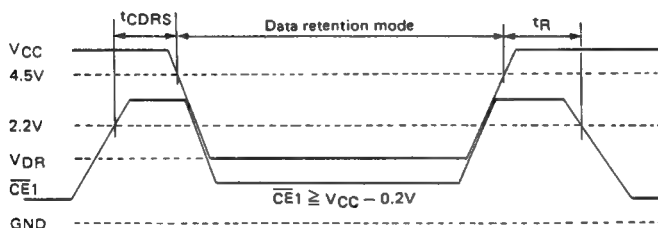


During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

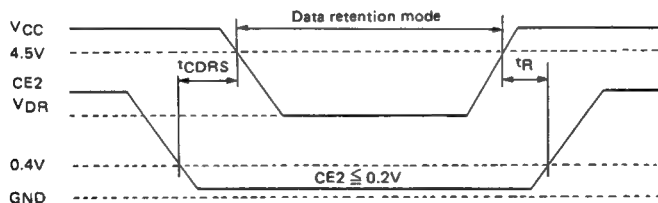
Data Retention Characteristics

(Ta=0 to +70 °C)

Item	Symbol	Test condition	- 25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V _{DR}	* 1	2.0	5.0	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V * 1	—	0.5	50	μA
	I _{CCDR2}	V _{CC} =2.0 to 5.5V * 1	—	1.0	100	μA
Data retention set up time	t _{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t _R		t _{RC} * 2	—	—	ns

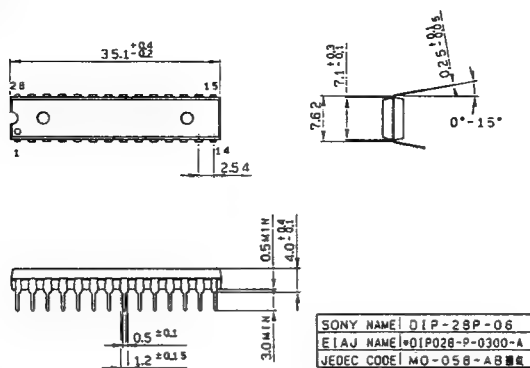
* 1 $\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$ * 2 t_{RC}: Read cycle timeData Retention Waveform (1): $\overline{CE1}$ control

Data Retention Waveform (2): CE2 control

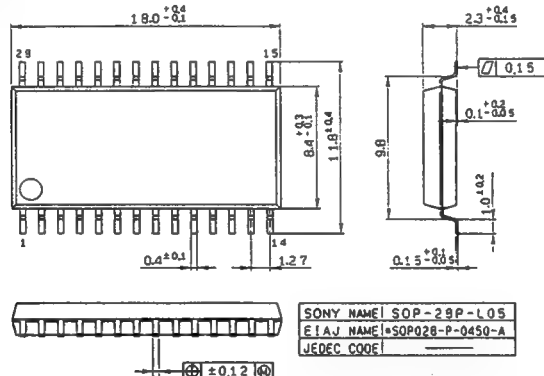


Package Outline Unit: mm

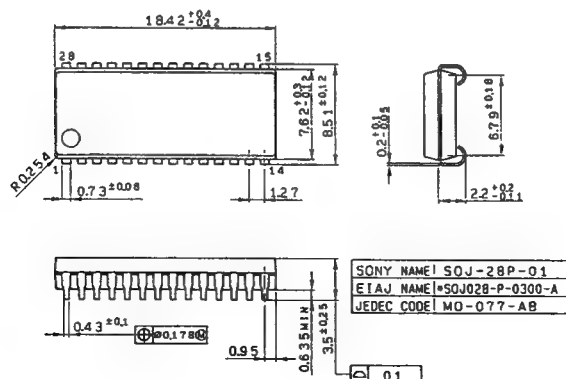
CXK5863BP 28pin DIP (Plastic) 300mil 2.0g



CXK5863BM 28pin SOP (Plastic) 450mil 0.7g



CXK5863BJ 28pin SOJ (Plastic) 300mil 0.8g

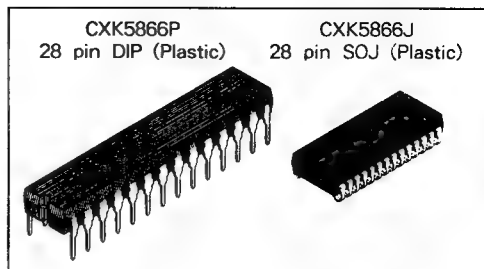


Description

The CXK5866P/J is a high speed CMOS static RAM which consists of 8,192-word × 8-bit. It operates at 15ns and 20ns high speed from 5V single power supply.

Features

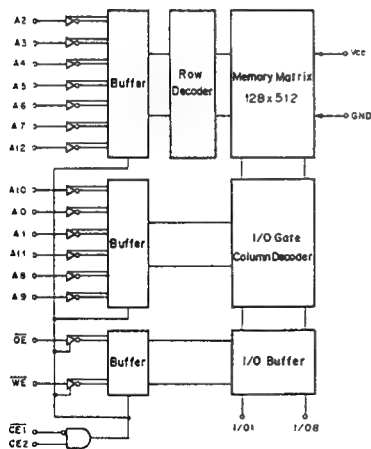
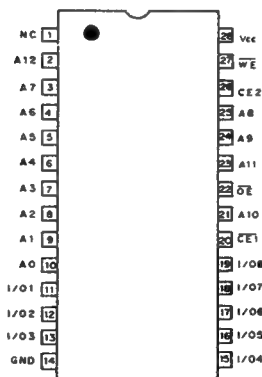
- High speed, low power consumption :
Access time Power consumption
(Max.) (Typ., Cycle=Min.)
CXK5866P/J-15 15ns 400mW
CXK5866P/J-20 20ns 325mW
- Single +5V power supply : $5V \pm 10\%$
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output :
three state output.
- Directly TTL compatible all inputs and outputs.
- Available in 28 pin 300mil DIP, 300mil SOJ package.


Function

8,192-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram

Pin Configuration
(Top view)

Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.**Truth Table**

$\overline{CE1}$	CE2	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics (V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _I	V _{IN} = GND to V _{CC}	-1	—	-1	μA
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , CE1 = V _{IH} or CE2 = V _{IL} , or OE = V _{IH} or WE = V _{IL}	-1	—	-1	μA
Operating power supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	—	—	
Average operating current	I _{CC2}	Cycle = Min, Duty = 100%, I _{OUT} = 0mA	-15	80	120	mA
			-20	65	100	
Standby current	I _{SB1}	CE1 ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	1	mA
	I _{SB2}	CE1 = V _{IH} or CE2 = V _{IL} , V _{IN} = V _{IH} /V _{IL} , Cycle = Min.	—	15	25	
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	6	pF

Note) This parameter is sampled and is not 100% tested.

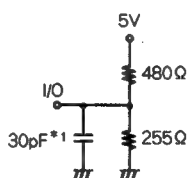
AC characteristics

• AC test conditions

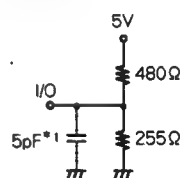
(V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 3ns
Input fall time	t _f = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



*1. including scope and jig capacitance

*2. for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	15	—	20	—	ns
Address access time	t _{AA}	—	15	—	20	ns
Chip enable access time (CE1)	t _{CO1}	—	15	—	20	ns
Chip enable access time (CE2)	t _{CO2}	—	15	—	20	ns
Output enable to output valid	t _{OE}	—	8	—	10	ns
Output hold from address change	t _{OH}	5	—	5	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} *, t _{LZ2} *	5	—	5	—	ns
Output enable to output in low Z (OE)	t _{OLZ} *	2	—	2	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	0	8	0	9	ns
Output disable to output in high Z (OE)	t _{OHZ} *	0	7	0	8	ns
Chip enable to power up time (CE1, CE2)	t _{PU}	0	—	0	—	ns
Chip disable to power down time (CE1, CE2)	t _{PD}	—	15	—	20	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

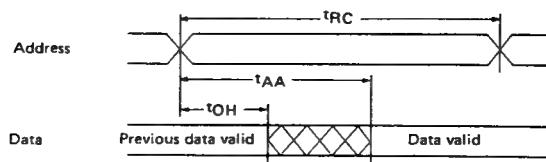
• Write cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	15	—	20	—	ns
Address valid to end of write	t _{AW}	12	—	14	—	ns
Chip enable to end of write	t _{CW}	12	—	14	—	ns
Data to write time overlap	t _{DW}	9	—	10	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	11	—	13	—	ns
Address set up time	t _{AS}	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	t _{WR}	0	—	0	—	ns
Write recovery time ($\overline{\text{CE1}}$, CE2)	t _{WR1}	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	7	0	9	ns

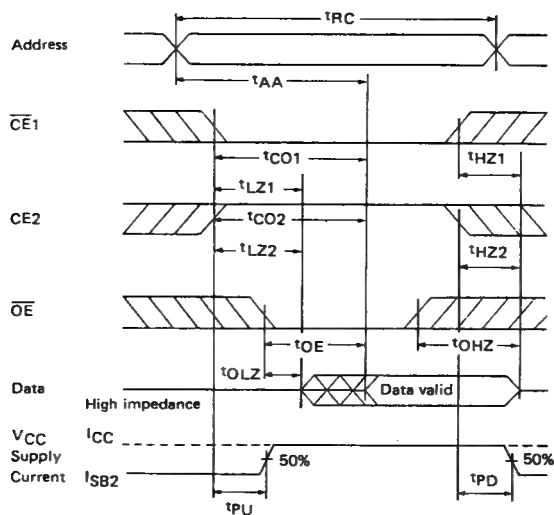
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

Timing Waveform

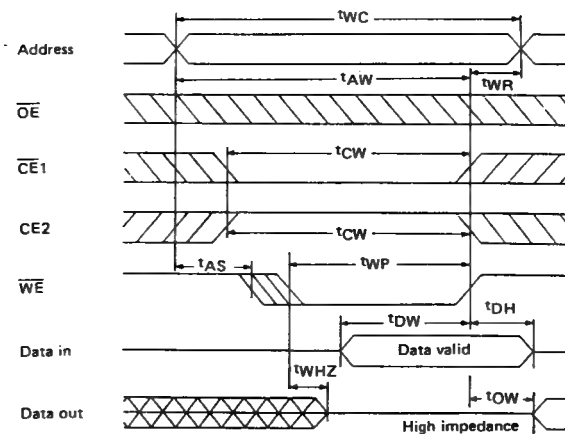
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



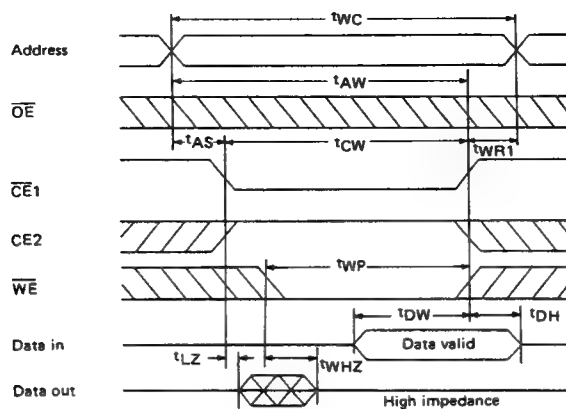
- Read cycle (2) : $\overline{WE} = V_{IH}$



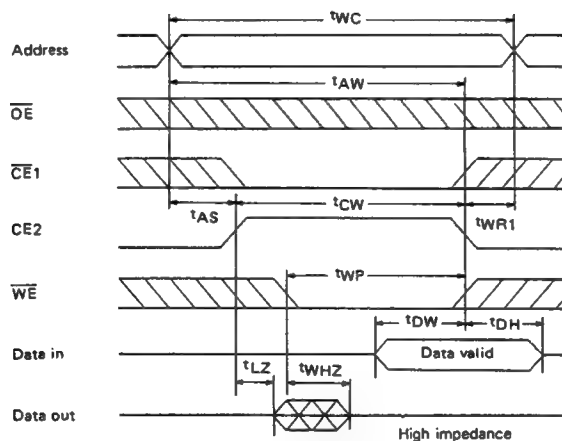
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control

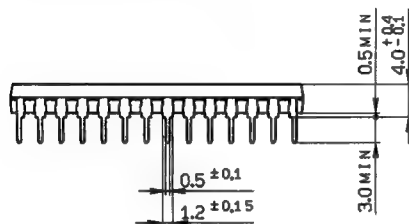
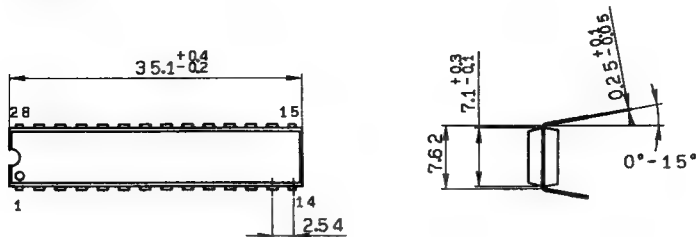


* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

CXK5866P

28pin DIP (Plastic) 300mil 2.0g

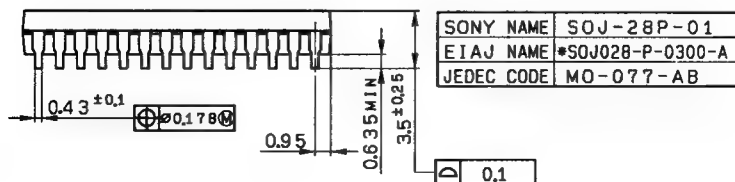
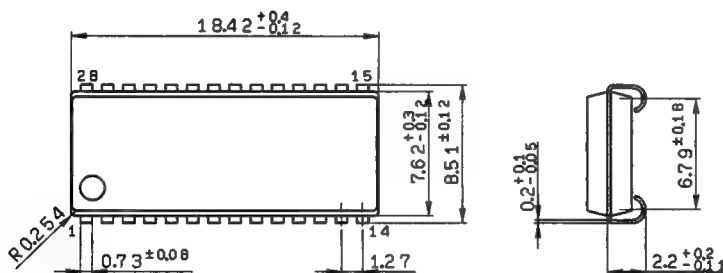


SONY NAME	DIP-28P-06
EIAJ NAME	*DIP028-P-0300-A
JEDEC CODE	MO-058-AB*

* (Similar)

CXK5866J

28pin SOJ (Plastic) 300mil 0.8g



SONY NAME	SOJ-28P-01
EIAJ NAME	*SOJ028-P-0300-A
JEDEC CODE	MO-077-AB

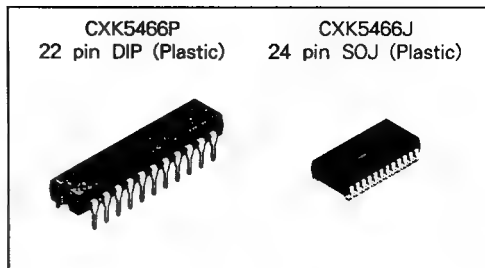
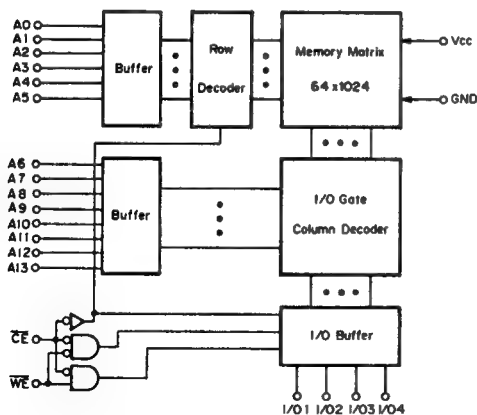
16,384 word × 4-bit High Speed CMOS Static RAM
Description

CXK5466P/J is a high speed CMOS static RAM with TTL compatible I/O organized as 16,384 words × 4 bits.

This IC operating on a single 5V supply turns to power down mode at no select time by means of chip enable signal.

Features

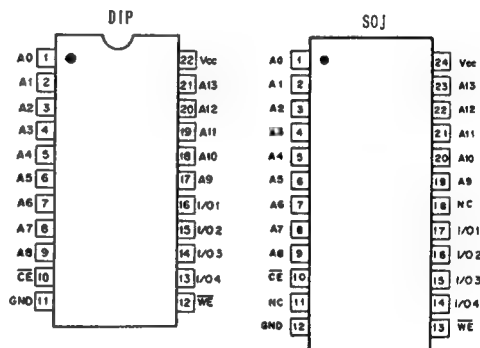
- Fast access time :
CXK5466P/J-15 15ns (Max.)
CXK5466P/J-20 20ns (Max.)
- Low power consumption : 150mW (Typ.)
During operation
- Single +5V supply : +5V ± 10 %
- Fully static memory
...No clock or timing strobe required
- Equal access and cycle time
- Common data input and output :
three-state output
- Directly TTL compatible :
All inputs and outputs
- Compatible with various types of packages
- High density : 300 mil 22 pin plastic DIP
300 mil 24 pin plastic SOJ

Block Diagram

Functions

16,384 word × 4-bit static RAM

Structure

Silicon gate CMOS IC

Pin Configuration (Top View)

Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input/output
CE	Chip enable input
WE	Write enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} Min. = - 3.5V for pulse width less than 20ns.**Truth Table**

\overline{CE}	\overline{WE}	Mode	I/O1 to I/O4	V _{CC} current
H	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	Read	Data output	I _{CC1} , I _{CC2}
L	L	Write	Data input	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*2	—	0.8	V

* 1) V_{CC} = 5V, Ta = 25°C* 2) V_{IL} Min. = - 3.0V for pulse width less than 20ns.

DC Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	Min.	Typ.*	Max.	Unit
Input leak current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	1	μA
Output leak current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{I/O} = GND to V _{CC}	-1	—	1	μA
Operating power supply current	I _{CC1}	$\overline{CE} = V_{IL}$, I _{OUT} = 0mA, V _{IN} = V _{IH} or V _{IL}	—	30	55	mA
Average operating current	I _{CC2}	Cycle = Min., Duty = 100%, I _{OUT} = 0mA	-15	—	95	mA
			-20	—	90	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} $\geq V_{CC} - 0.2V$ or V _{IN} $\leq 0.2V$	—	—	1	mA
	I _{SB2}	$\overline{CE} = V_{IH}$, V _{IN} = V _{IH} /V _{IL} Cycle = Min.	—	—	85	mA
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5.0V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Input/output capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

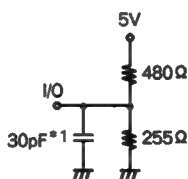
AC characteristics

• AC test conditions

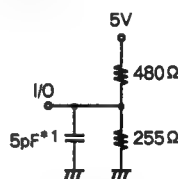
(V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



*1 including scope and jig capacitance

*2 for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	trc	15	—	20	—	ns
Address access time	tAA	—	15	—	20	ns
Chip enable access time (CE)	tco	—	15	—	20	ns
Output hold from address change	toH	3	—	3	—	ns
Chip enable to output in low Z (CE)	tlZ *	2	—	3	—	ns
Chip disable to output in high Z	thZ *	0	6	0	8	ns
Chip enable to power up time	tpu	0	—	0	—	ns
Chip disable to power down time	tpd	—	15	—	20	ns

* Transition is tested by means of load conditions (2), from stationary condition at $\pm 200\text{mV}$
(See Fig. 1)

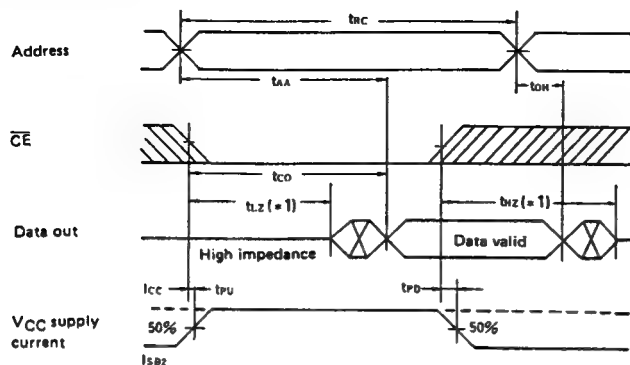
• Write cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	tWC	15	—	20	—	ns
Address valid to end of write	tAW	13	—	18	—	ns
Chip enable to end of write	tCW	13	—	18	—	ns
Data to write time overlap	tdW	8	—	11	—	ns
Data hold from write time	tdH	0	—	0	—	ns
Write pulse width	tWP	13	—	18	—	ns
Address setup time	tAS	0	—	0	—	ns
Write recovery time	tWR	0	—	0	—	ns
Output active from end of write	tOW *	2	—	3	—	ns
Write to output in high Z	tWHZ *	0	5	0	7	ns

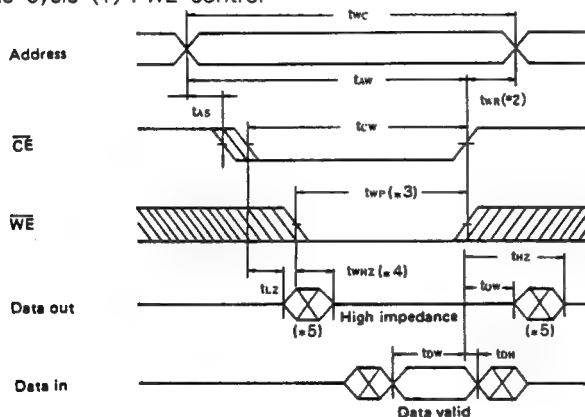
* Transition is tested by means of load conditions (2), from stationary condition at $\pm 200\text{mV}$
(See Fig. 1)

Timing Waveform

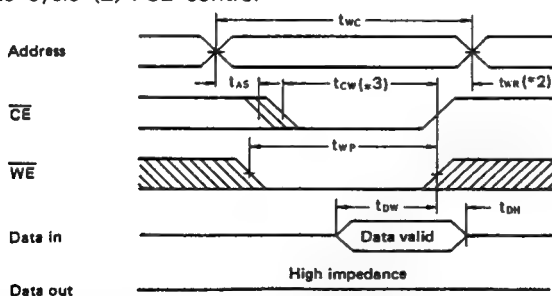
- Read cycle : $\overline{WE} = V_{IH}$



- Write cycle (1) : \overline{WE} control



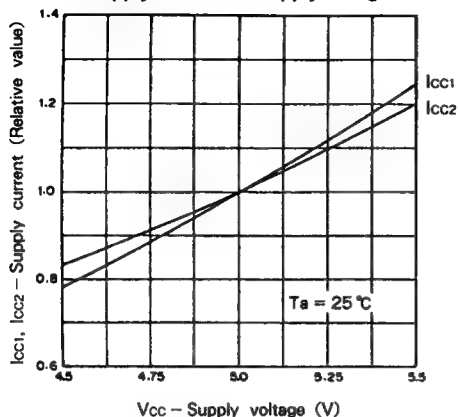
- Write cycle (2) : \overline{CE} control



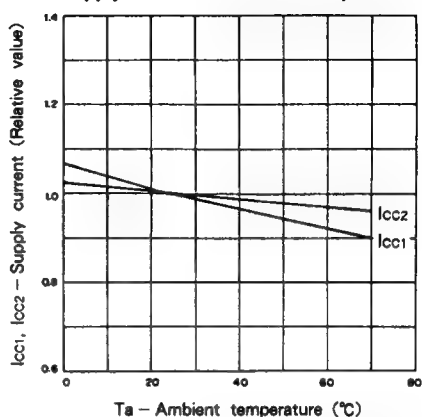
- *1) Whatever the conditions, t_{HZ} is smaller than t_{LZ} .
- *2) t_{WR} is tested from either \overline{CE} or \overline{WE} rise, whichever comes earlier, until the end of write cycle.
- *3) Write is performed when both \overline{CE} and \overline{WE} are in the low overlap.
- *4) When \overline{WE} fall is performed simultaneously with \overline{CE} fall, or before, output is kept to high impedance.
- *5) While I/O pins are in output state, do not apply data input signals with a phase opposite to that of the output.

Example of Representative Characteristics

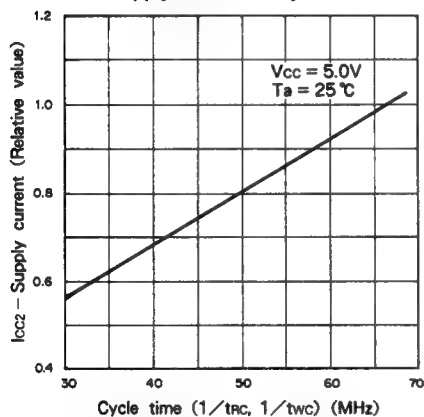
Supply current vs. Supply voltage



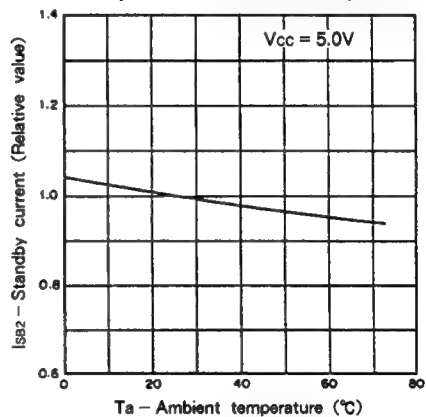
Supply current vs. Ambient temperature



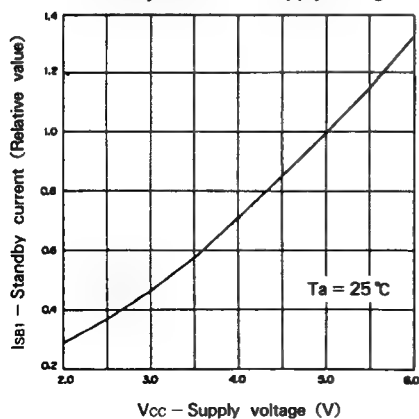
Supply current vs. Cycle time



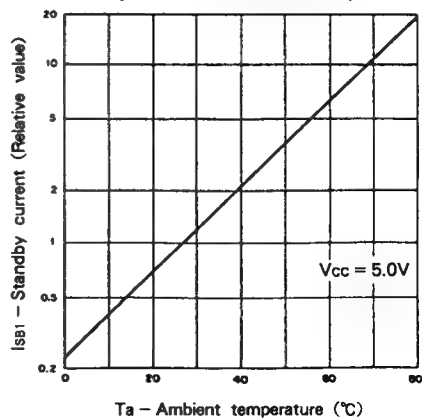
Standby current vs. Ambient temperature



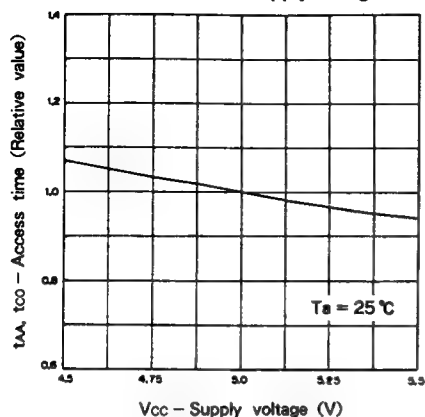
Standby current vs. Supply voltage



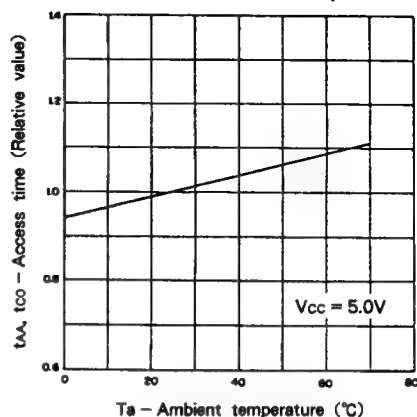
Standby current vs. Ambient temperature



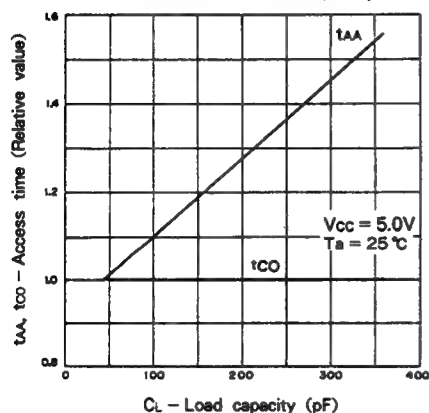
Access time vs. Supply voltage



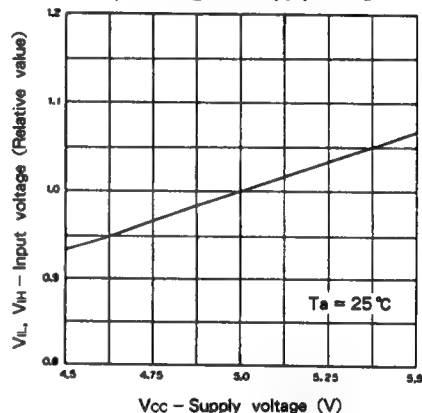
Access time vs. Ambient temperature



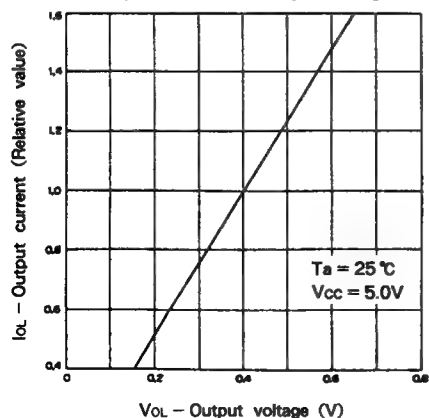
Access time vs. Load capacity



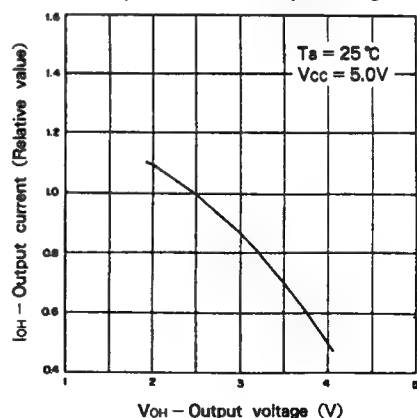
Input voltage vs. Supply voltage



Output current vs. Output voltage



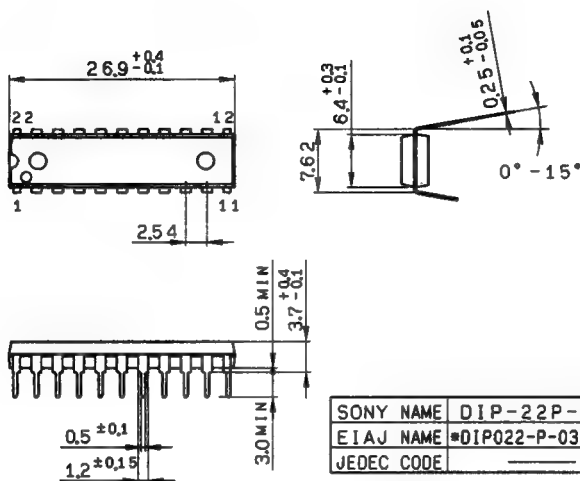
Output current vs. Output voltage



Package Outline Unit : mm

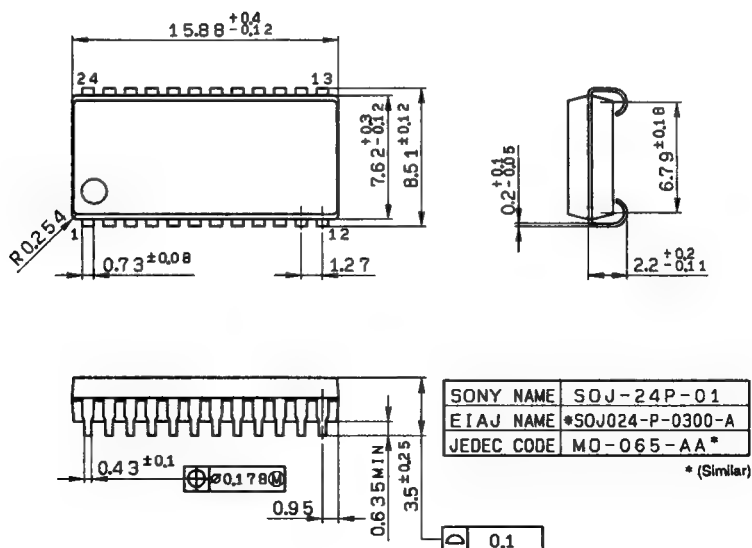
CXK5466P

22 pin DIP (Plastic) 300mil 1.3g



CXK5466J

24 pin SOJ (Plastic) 300mil 0.7g



16,384 word × 4-bit High Speed CMOS Static RAM
Description

CXK5467P/J is a high speed CMOS static RAM with TTL compatible I/O organized as 16,384 words × 4 bits.

This IC operating on a single 5V supply turns to power down mode at no select time by means of chip enable signal. An output enable pin controls the output.

Features

- Fast access time :
CXK5467P/J-15 15ns (Max.)
CXK5467P/J-20 20ns (Max.)
- Low power consumption : 150mW (Typ.)
During operation
- Single +5V supply : +5V ± 10 %
- Fully static memory
...No clock or timing strobe required
- Output Enable (OE) control available
- Equal access and cycle time
- Common data input and output :
three-state output
- Directly TTL compatible : All inputs and outputs
- Compatible with various types of packages
- High density : 300 mil 24 pin plastic DIP
300 mil 24 pin plastic SOJ

CXK5467P
24 pin DIP (Plastic)



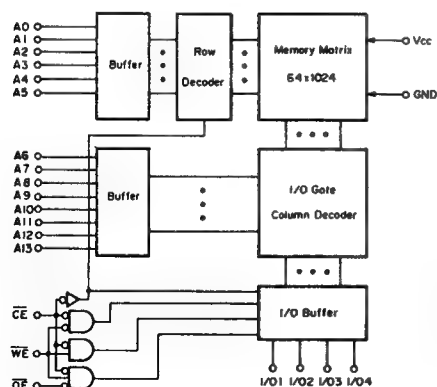
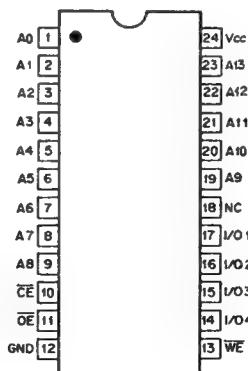
CXK5467J
24 pin SOJ (Plastic)


Functions

16,384 word × 4-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram

**Pin Configuration
(Top View)**

Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} Min. = - 3.5V for pulse width less than 20ns.**Truth Table**

\overline{CE}	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O4	V _{CC} current
H	x	x	Not selected	High Z	I _{sB1} , I _{sB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data output	I _{CC1} , I _{CC2}
L	x	L	Write	Data input	I _{CC1} , I _{CC2}

x : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*2	—	0.8	V

*1) V_{CC} = 5V, Ta = 25°C*2) V_{IL} Min. = - 3.0V for pulse width less than 20ns.

DC Electrical Characteristics

● DC and operating characteristics

(V_{CC} = 5V ± 10 %, GND = 0V, T_a = 0 to +70 °C)

Item	Symbol	Test Conditions	Min.	Typ.*	Max.	Unit
Input leak current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	1	μA
Output leak current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{I/O} = GND to V _{CC}	-1	—	1	μA
Operating power supply current	I _{CC1}	$\overline{CE} = V_{IL}$, I _{OUT} = 0mA, V _{IN} = V _{IH} or V _{IL}	—	30	55	mA
Average operating current	I _{CC2}	Cycle = Min., Duty = 100 %, I _{OUT} = 0mA	-15	—	95	mA
			-20	—	90	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	1	mA
	I _{SB2}	$\overline{CE} = V_{IH}$, V _{IN} = V _{IH} /V _{IL} Cycle = Min.	—	—	85	mA
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5.0V, T_a = 25 °C

I/O capacitance

(T_a = 25 °C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Input/output capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100 % tested.

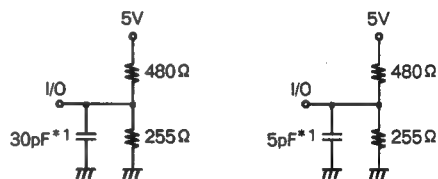
● AC test conditions

(V_{CC} = 5V ± 10 %, T_a = 0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)

Output Load (2)*2



*1 including scope and jig capacitance

*2 for t_{LZ}, t_{OLZ}, t_{HZ}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	15	—	20	—	ns
Address access time	t _{AA}	—	15	—	20	ns
Chip enable access time (\overline{CE})	t _{CO}	—	15	—	20	ns
Output enable to output valid	t _{OE}	—	8	—	10	ns
Output hold from address change	t _{OH}	3	—	3	—	ns
Chip enable to output in low Z (\overline{CE})	t _{LZ} *	2	—	3	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ} *	2	—	3	—	ns
Chip disable to output in high Z	t _{HZ} *	0	6	0	8	ns
Output disable to output in high Z (\overline{OE})	t _{OHZ} *	0	6	0	8	ns
Chip enable to power up time	t _{PU}	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	15	—	20	ns

* Transition is tested by means of load conditions (2), from stationary condition at $\pm 200\text{mV}$ (See Fig. 1)

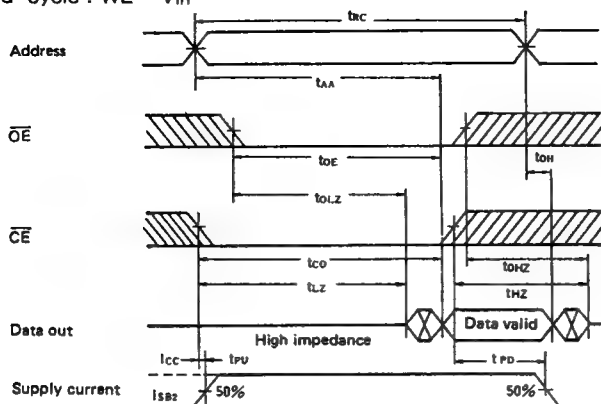
• Write cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	15	—	20	—	ns
Address valid to end of write	t _{AW}	13	—	18	—	ns
Chip enable to end of write	t _{CW}	13	—	18	—	ns
Data to write time overlap	t _{DW}	8	—	11	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	13	—	18	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	ns
Output active from end of write	t _{OW} *	2	—	3	—	ns
Write to output in high Z	t _{WHZ}	0	5	0	7	ns

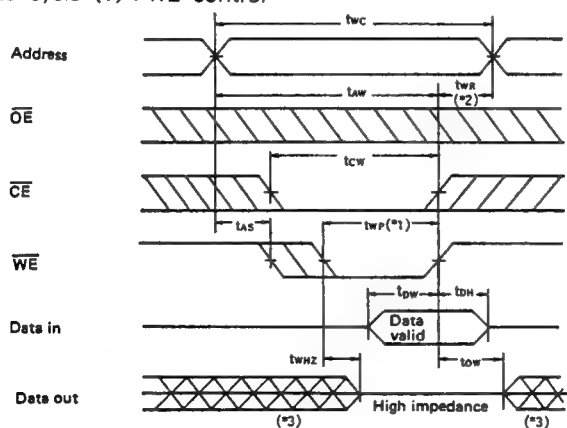
* Transition is tested by means of load conditions (2), from stationary condition at $\pm 200\text{mV}$ (See Fig. 1)

Timing Waveform

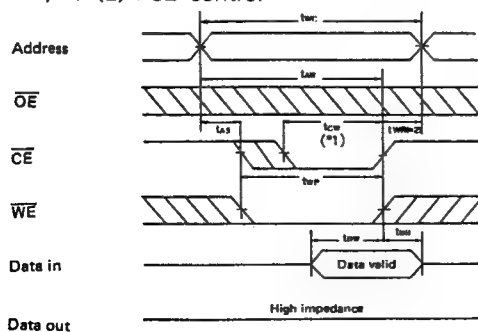
• Read cycle : $\overline{WE} = V_{IH}$



• Write cycle (1) : \overline{WE} control



• Write cycle (2) : \overline{CE} control



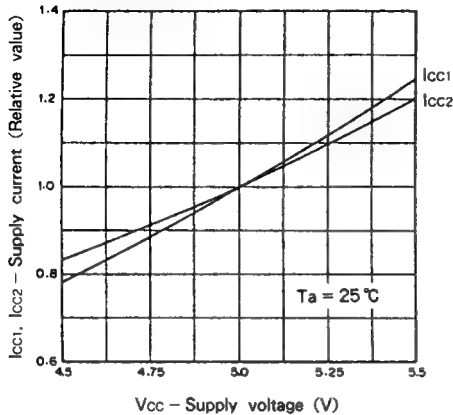
*1) Write is performed during the low overlap of \overline{CE} and \overline{WE} .

*2) t_{WH} is measured from the rising of either \overline{CE} or \overline{WE} , whichever is earlier, to the end of write cycle.

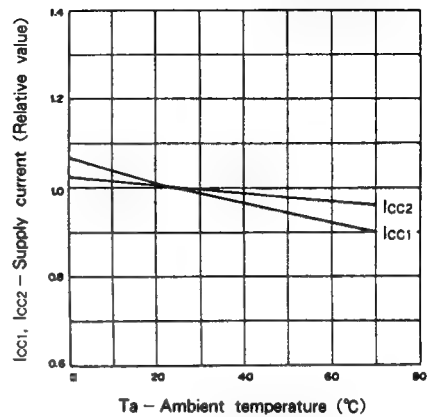
*3) While I/O pins are in output state, a data input voltage of a phase opposite to the output must not be applied.

Example of Representative Characteristics

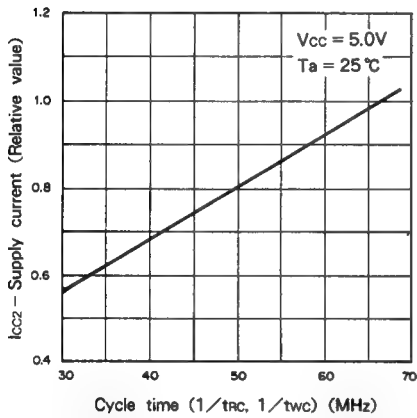
Supply current vs. Supply voltage



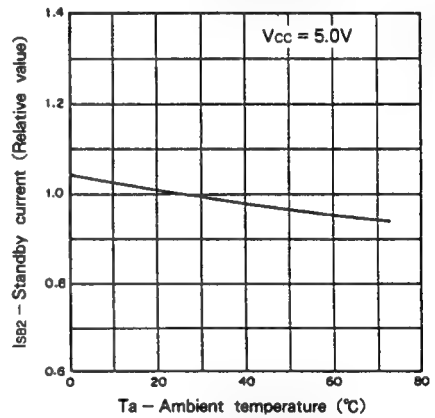
Supply current vs. Ambient temperature



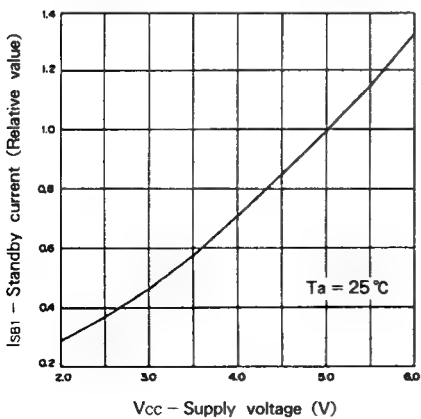
Supply current vs. Cycle time



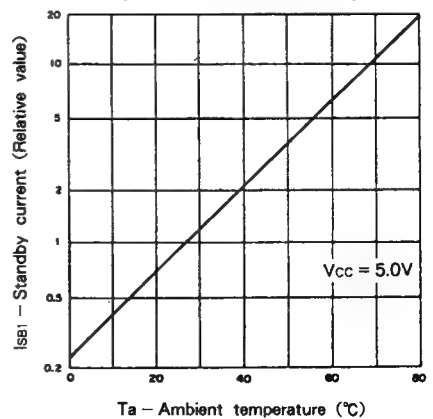
Standby current vs. Ambient temperature



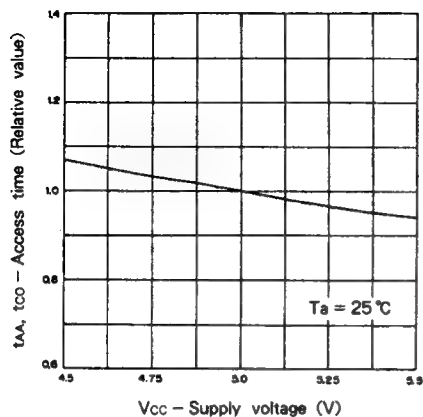
Standby current vs. Supply voltage



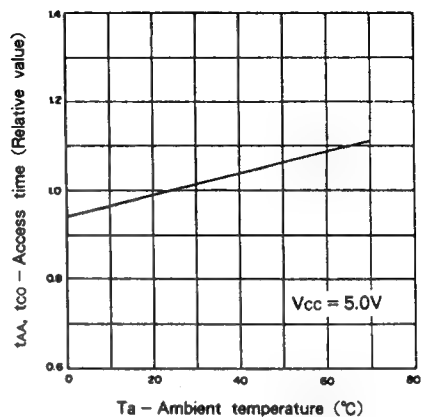
Standby current vs. Ambient temperature



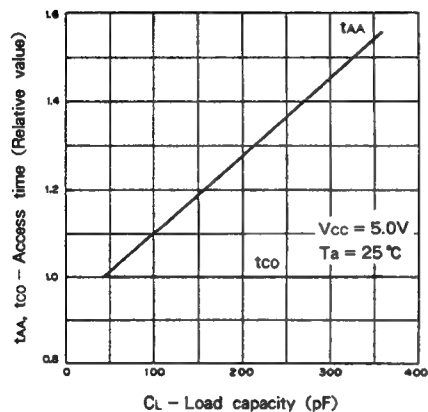
Access time vs. Supply voltage



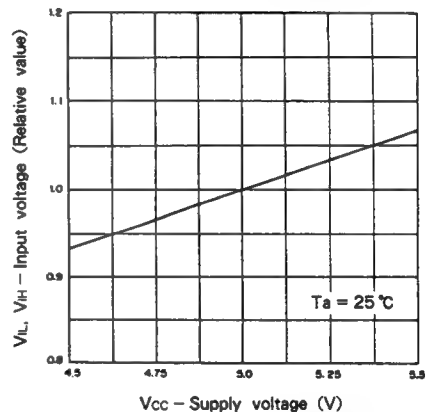
Access time vs. Ambient temperature



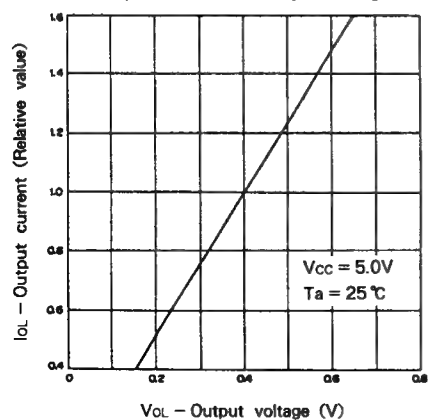
Access time vs. Load capacity



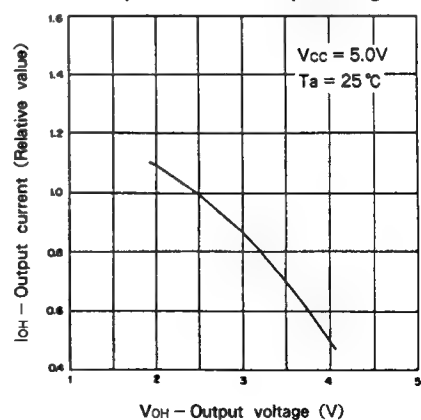
Input voltage vs. Supply voltage



Output current vs. Output voltage

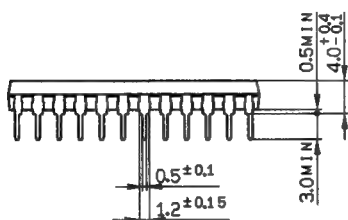
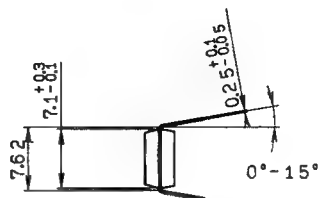
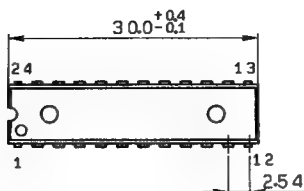


Output current vs. Output voltage



Package Outline Unit : mm

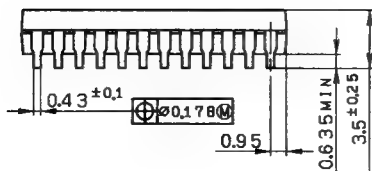
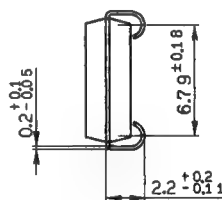
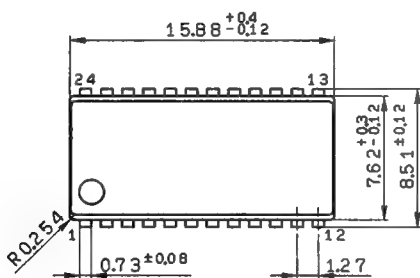
CXK5467P 24pin DIP (Plastic) 300mil 1.5g



SONY NAME	DIP-24P-08
EIAJ NAME	*DIP024-P-0300-B
JEDEC CODE	MO-058-AA *

* (Similar)

CXK5467J 24pin SOJ (Plastic) 300mil 0.7g



SONY NAME	SOJ-24P-01
EIAJ NAME	*SOJ024-P-0300-A
JEDEC CODE	MO-065-AA *

* (Similar)

D 0.1

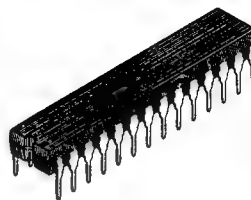
Description

CXK5971AP/AM/AJ are 73,728 bits high speed CMOS static RAMs organized as 8,192-word by 9-bit and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time 25ns/30ns/35ns (Max.)
- Low power standby 5 μ W (Typ.)
- Low power operation 300mW (Typ., Cycle=Min.)
- Single + 5V supply: 5V \pm 10%
- Fully static memory... No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three state output.
- Directly TTL compatible: all inputs and outputs.
- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin 300mil DIP, 450mil SOP, and 300mil SOJ.

CXK5971AP
28 pin DIP (Plastic)



CXK5971AM
28 pin SOP (Plastic)



CXK5971AJ
28 pin SOJ (Plastic)



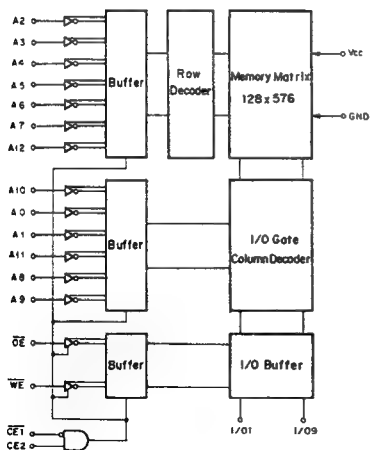
Function

8192-word × 9-bit static RAM

Structure

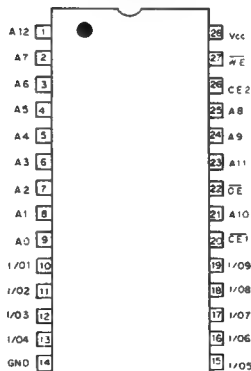
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O9	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V Power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 * to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK5971AP/AJ	1.0
		CXK5971AM	0.7
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature* time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O}=-3.5V Min. for pulse width less than 20ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O9	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL}=-3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70°C)

Item	Symbol	Test condition	- 25/30/35			Unit
			Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	-1	—	1	μA
Output leakage current	I _{LO}	V _{I/O} =GND to V _{CC} , CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL}	-1	—	1	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	—	—	—	mA
Average operating current	I _{CC2}	Cycle=Min, Duty=100%, I _{OUT} =0mA	—	60	90	mA
Standby current	I _{SB1}	CE1 ≥ V _{CC} -0.2V or CE2 ≤ 0.2V V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	—	1	100	μA
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL} , V _{IN} =V _{IH} /V _{IL} , Cycle=Min.	—	10	25	mA
Output high voltage	V _{OH}	I _{OH} =-4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =8.0mA	—	—	0.4	V

* V_{CC}=5V, T_a=25°C

I/O Capacitance

(T_a=25°C, f=1MHz)

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	6	pF

Note) This parameter is sampled and is not 100% tested.

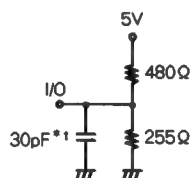
AC Characteristics

● AC test conditions

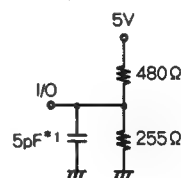
(V_{CC}=5V ± 10%, T_a=0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} =3.0V
Input pulse low level	V _{IL} =0V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2) *2



* 1. including scope and jig capacitance

* 2. for tLZ1, tLZ2, tOLZ, tHZ1, tHZ2, tOHZ, tOW, tWH2

Fig. 1

• Read cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	25	—	30	—	35	ns
Chip enable access time (CE2)	t _{CO2}	—	25	—	30	—	35	ns
Output enable to output valid	t _{OE}	—	12	—	12	—	15	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t _{LLZ} * t _{LLZ} *	5	—	5	—	5	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t _{HZ1} * t _{HZ2} *	0	12	0	12	0	15	ns
Chip disable to output in high Z (\overline{OE})	t _{OHZ} *	0	10	0	10	0	12	ns
Chip enable to power up time (CE1, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time ($\overline{CE1}$, CE2)	t _{PD}	—	20	—	20	—	20	ns

• Write cycle

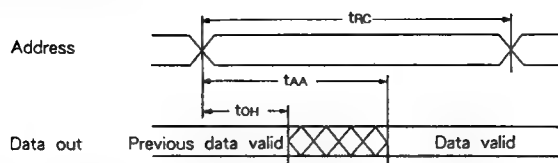
Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	20	—	20	—	30	—	ns
Chip enable to end of write	t _{CW}	20	—	20	—	30	—	ns
Data to write time overlap	t _{DW}	12	—	12	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	20	—	20	—	25	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	12	0	12	0	15	ns

* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

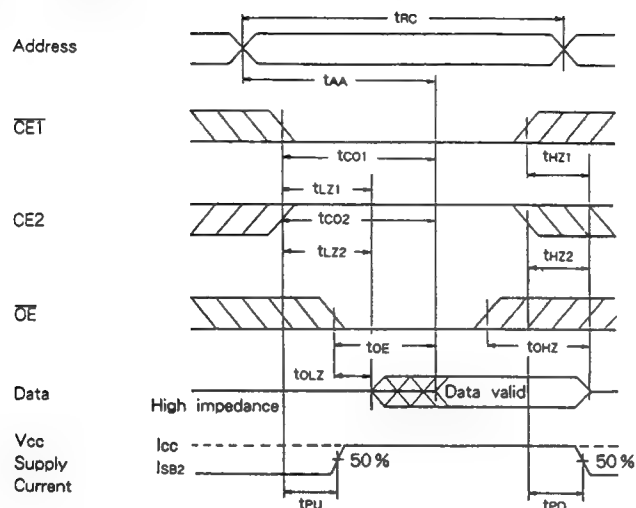
This parameter is sampled and is not 100% tested.

Timing Waveform

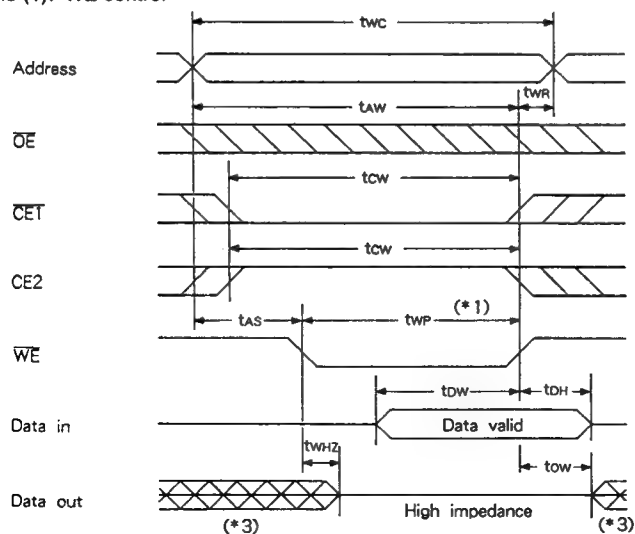
- Read cycle (1): $\overline{CE1}=\overline{OE}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



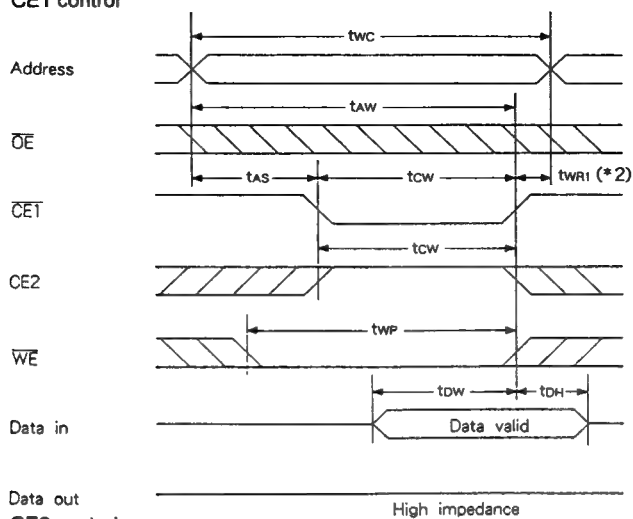
- Read cycle (2): $\overline{WE}=V_{IH}$



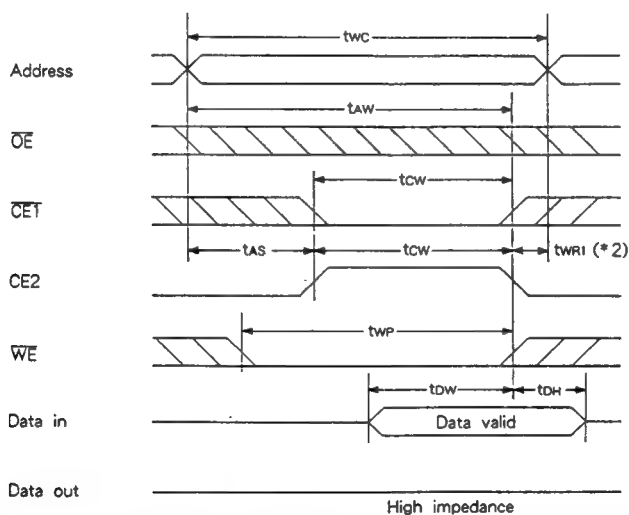
- Write cycle (1): \overline{WE} control



- Write cycle (2): $\overline{\text{CE1}}$ control



- **Write cycle (3): CE2 control**



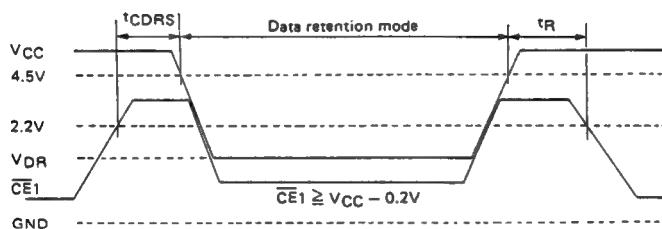
Note)

- *1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- *2. tw_{WT} is tested from either the rising edge of CE1 or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.
- *3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

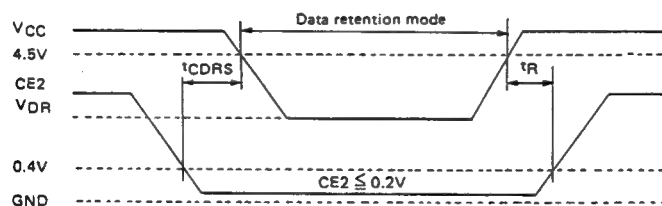
Data Retention Characteristics

(Ta=0 to +70 °C)

Item	Symbol	Test condition	- 25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1	2.0	5.0	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V *1	—	0.5	50	μA
	I _{CCDR2}	V _{CC} =2.0 to 5.5V *1	—	1.0	100	μA
Data retention set up time	t _{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t _R		t _{RC} *2	—	—	ns

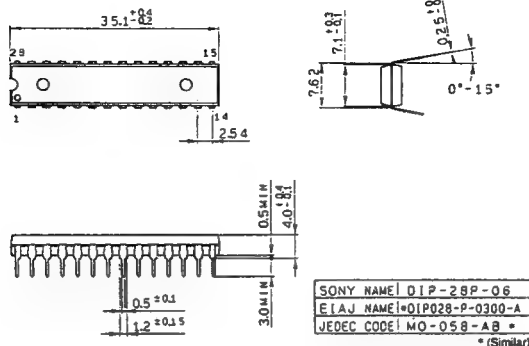
*1 $\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$ *2 t_{RC}: Read cycle timeData Retention Waveform (1): $\overline{CE1}$ control

Data Retention Waveform (2): CE2 control

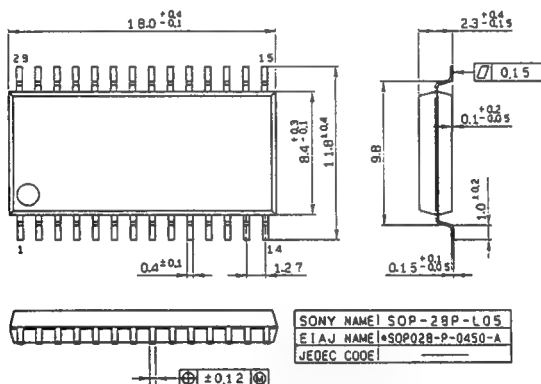


Package Outline Unit : mm

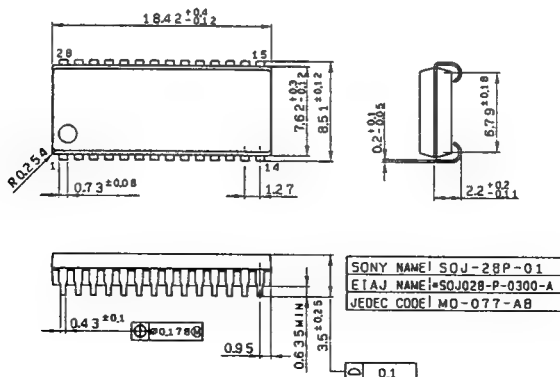
CXK5971AP 28pin DIP (Plastic) 300mil 2.0g



CXK5971AM 28pin SOP (Plastic) 450mil 0.7g



CXK5971AJ 28pin SOJ (Plastic) 300mil 0.8g



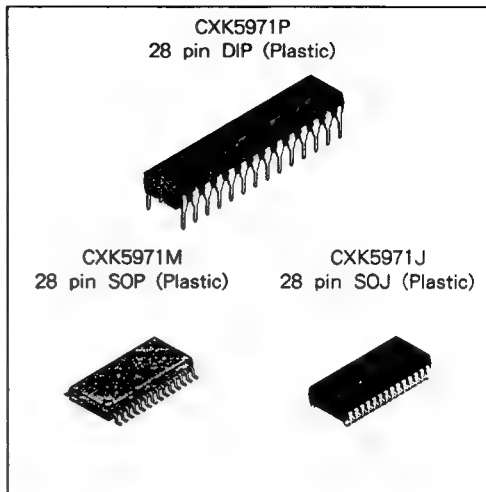
8192-word × 9-bit High Speed CMOS Static RAM

Description

CXK5971P/M/J are 73,728 bits high speed CMOS static RAMs organized as 8,192-word by 9-bit and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time 25ns/30ns/35ns (Max.)
- Low power standby 5 μ W (Typ.)
- Low power operation 150mW (Typ.)
- Single + 5V supply : 5V \pm 10 %
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Low voltage data retention 2.0V (Min.)
- Full CMOS.
- Available in 28 pin 300mil DIP, 450mil SOP and 300 mil SQJ.



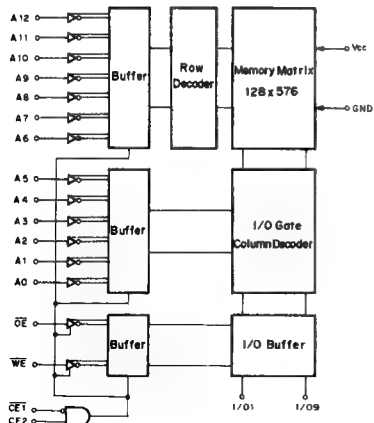
Structure

Silicon gate CMOS IC

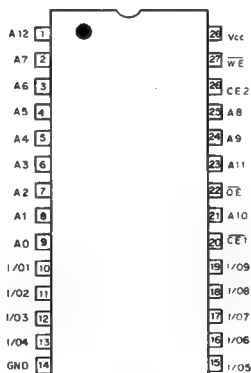
Function

8192-word X 9-bit static RAM

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O9	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V Power supply
GND	Ground

Absolute Maximum Ratings

Ta = 25°C, GND = 0V

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK5971P/J	1.0
		CXK5971M	0.7
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

*Note) V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O9	V _{CC} Current
H	X	X	X	Not selected	High Z	Isb1, Isb2
X	L	X	X	Not selected	High Z	Isb1, Isb2
L	H	H	H	Output disable	High Z	Icc1, Icc2
L	H	L	H	Read	Data out	Icc1, Icc2
L	H	X	L	Write	Data in	Icc1, Icc2

X: "H" or "L"

DC Recommended Operating Conditions

Ta = 0 to + 70°C, GND = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

*Note) V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

 $V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0$ to $+70^\circ C$

Item	Symbol	Test condition	- 25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	$V_{IN} = GND$ to V_{CC}	-1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O} = GND$ to V_{CC} , $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OUT} = 0mA$	—	30	60	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100 %, $I_{OUT} = 0mA$	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	1	100	μA
	I_{SB2}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH}	—	10	25	mA
Output high voltage	V_{OH}	$I_{OH} = -4.0mA$	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0mA$	—	—	0.4	V

* $V_{CC} = 5V$, $T_a = 25^\circ C$

I/O capacitance

 $T_a = 25^\circ C$, $f = 1MHz$

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF

(Note) This parameter is sampled and is not 100 % tested.

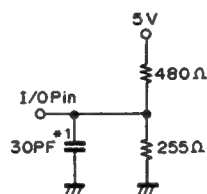
AC characteristics

● AC test conditions

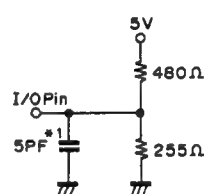
 $V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ C$

Item	Condition
Input pulse high level	$V_{IH} = 3.0V$
Input pulse low level	$V_{IL} = 0V$
Input rise time	$t_r = 5ns$
Input fall time	$t_f = 5ns$
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* 1. including scope and jig capacitance

* 2. for t_{LZ1} , t_{LZ2} , t_{OLZ} , t_{HZ1} , t_{HZ2} , t_{OHZ} , t_{OW} , t_{WHZ}

Fig. 1

1) Read cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{\text{CE1}}$)	t _{CO1}	—	25	—	30	—	35	ns
Chip enable access time (CE2)	t _{CO2}	—	25	—	30	—	35	ns
Output enable to output valid	t _{OE}	—	15	—	15	—	20	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{\text{CE1}}$, CE2)	t _{LEZ1} * t _{LEZ2} *	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{\text{CE1}}$, CE2)	t _{HZ1} * t _{HZ2} *	0	15	0	15	0	20	ns
Chip disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	0	13	0	13	0	15	ns
Chip enable to power up time ($\overline{\text{CE1}}$, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time ($\overline{\text{CE1}}$, CE2)	t _{PD}	—	20	—	20	—	20	ns

2) Write cycle

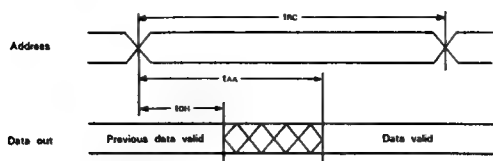
Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	20	—	20	—	30	—	ns
Chip enable to end of write	t _{CW}	20	—	20	—	30	—	ns
Data to write time overlap	t _{DW}	12	—	12	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	20	—	20	—	25	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{CE1}}$, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	13	0	13	0	15	ns

* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

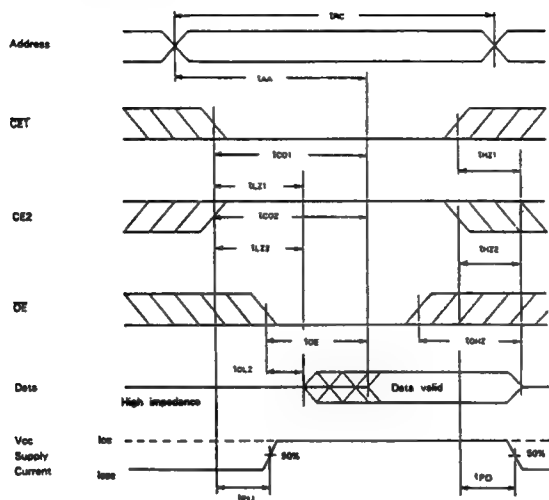
Timing Waveform

1) Read cycle

- Read cycle No. 1 : [$\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$]

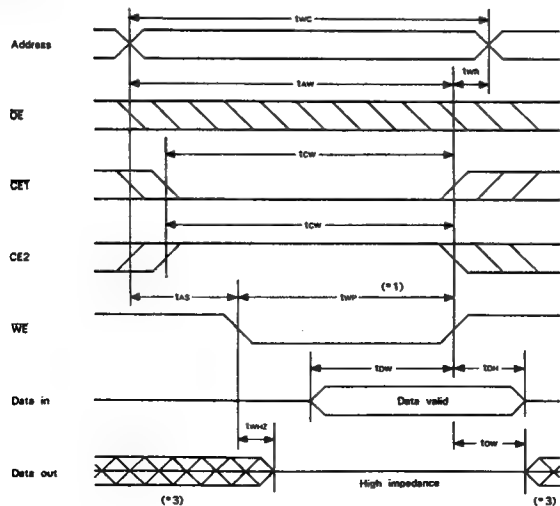


- Read cycle No. 2 : [$\overline{WE} = V_{IH}$]

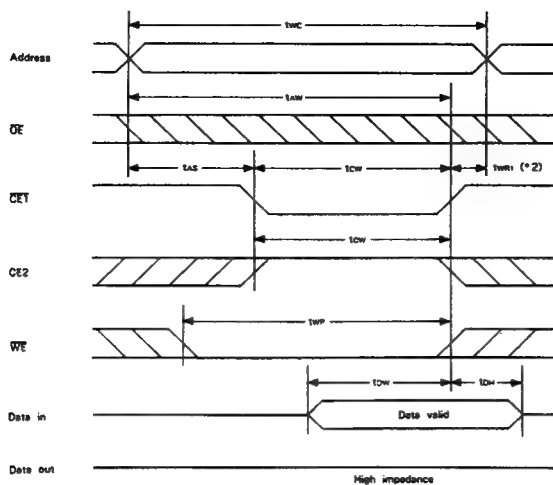


2) Write cycle

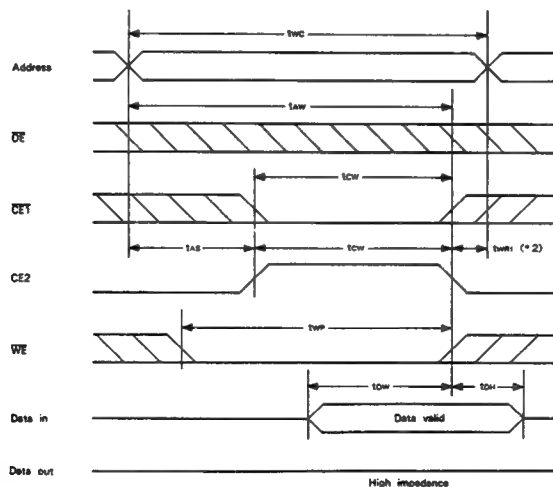
- Write cycle No. 1 : [\overline{WE} control]



• Write cycle No. 2 : [$\overline{\text{CE1}}$ control]



• Write cycle No. 3 : [CE2 control]



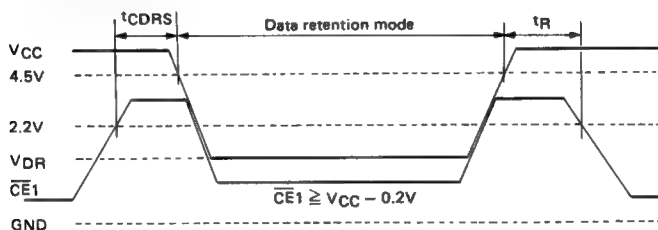
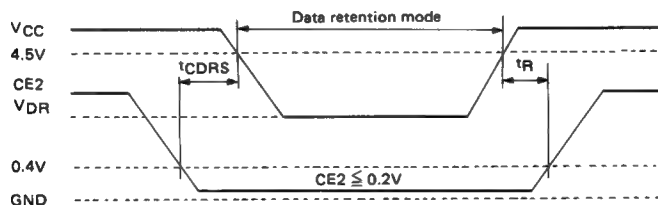
Note)

- *1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- *2. t_{WR1} is tested from either the rising edge of $\overline{\text{CE1}}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.
- *3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

Data Retention Characteristics

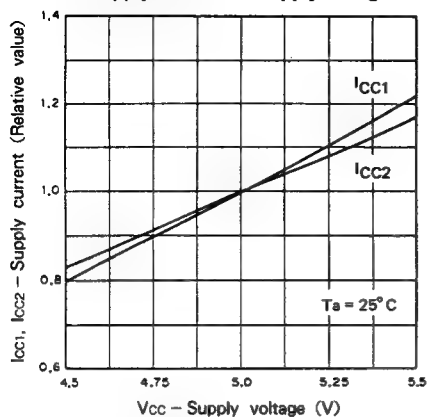
 $T_a = 0 \text{ to } +70^\circ\text{C}$

Item	Symbol	Test condition	- 25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0\text{V} *1$	—	0.5	50	μA
	I_{CCDR2}	$V_{CC} = 2.0 \text{ to } 5.5\text{V} *1$	—	1.0	100	μA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		$t_{RC} *2$	—	—	ns

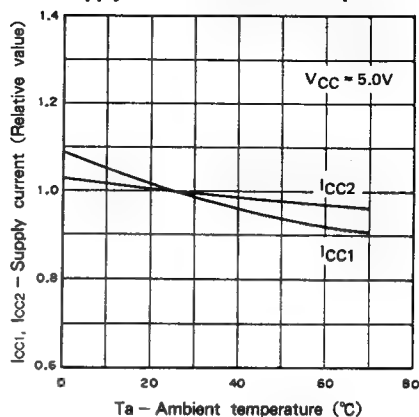
*1 $\overline{CE1} \geq V_{CC} - 0.2\text{V}$ or $\overline{CE2} \leq 0.2\text{V}$, $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$ *2 t_{RC} : Read cycle timeData Retention Waveform (1) : [$\overline{CE1}$ control]Data Retention Waveform (2) : [$\overline{CE2}$ control]

Example of Representative Characteristics

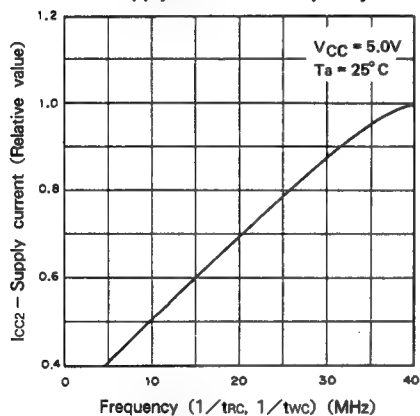
Supply current vs. Supply voltage



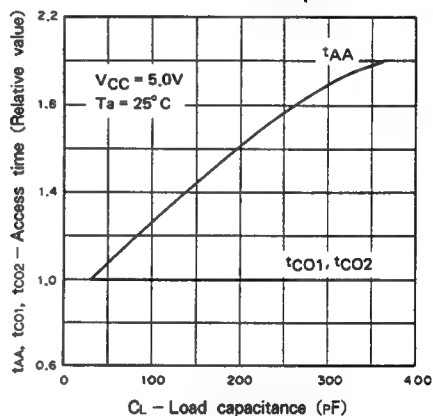
Supply current vs. Ambient temperature



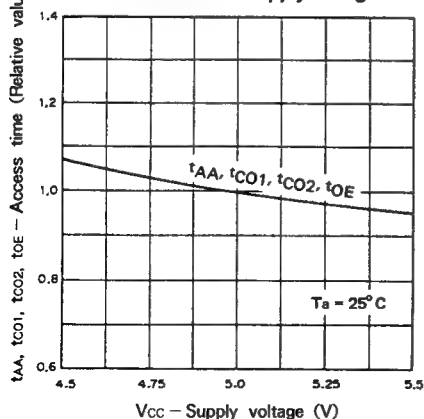
Supply current vs. Frequency



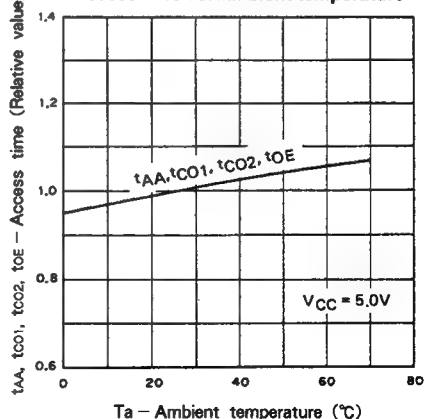
Access time vs. Load capacitance



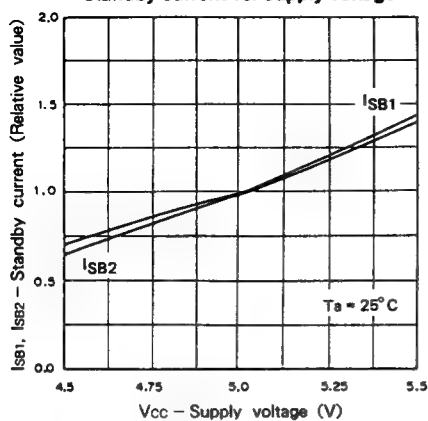
Access time vs. Supply voltage



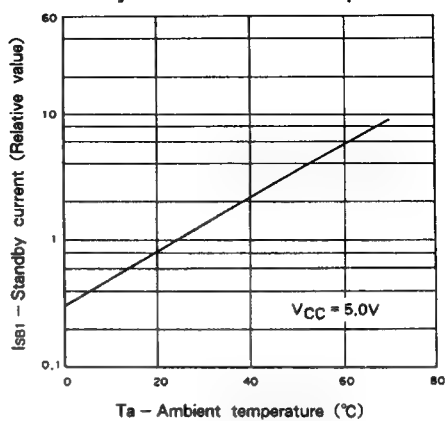
Access time vs. Ambient temperature



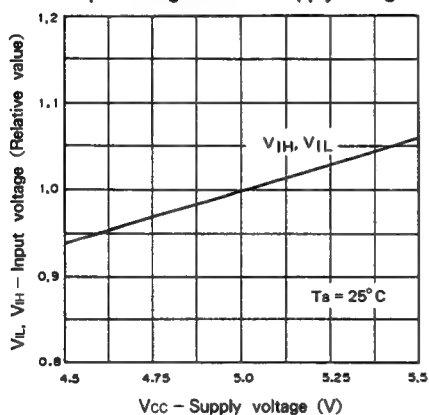
Standby current vs. Supply voltage



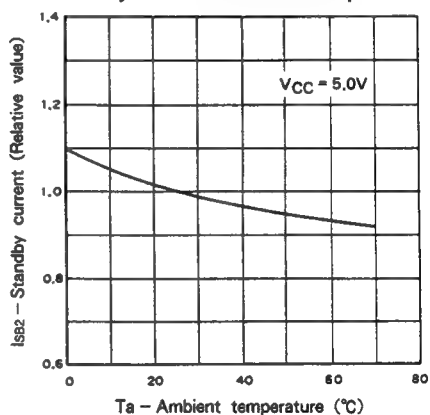
Standby current vs. Ambient temperature



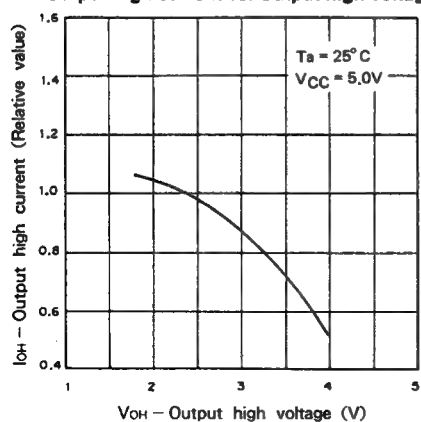
Input voltage level vs. Supply voltage



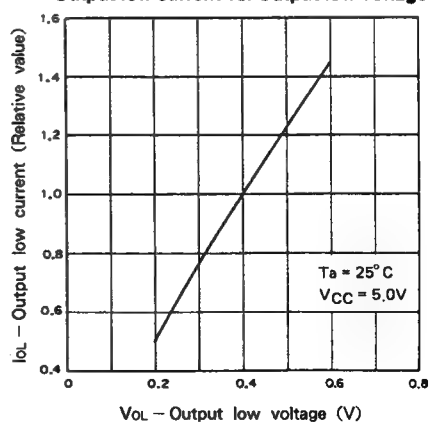
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

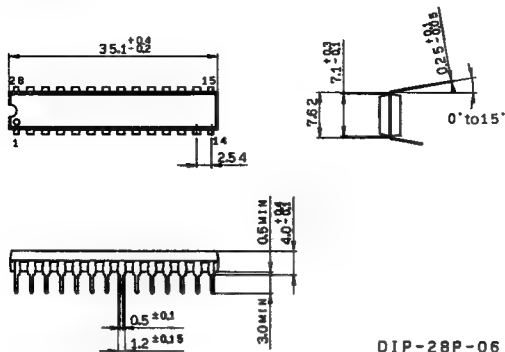


Output low current vs. Output low voltage



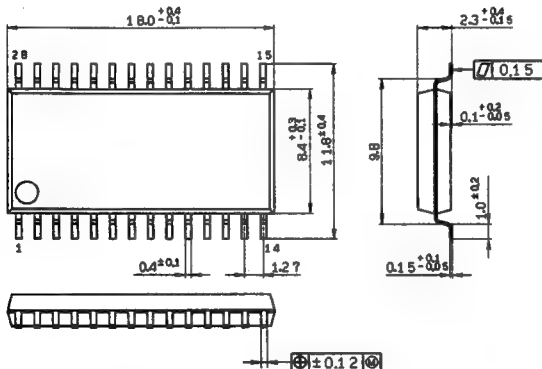
Package Outline Unit : mm

CXK5971P 28 pin DIP (Plastic) 300mil 2.0g



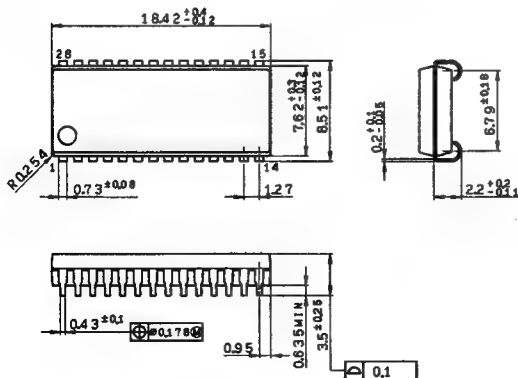
DIP-28P-06

CXK5971M 28 pin SOP (Plastic) 450mil 0.7g



SOP-28P-L05

CXK5971J 28 pin SOJ (Plastic) 300mil 0.8g



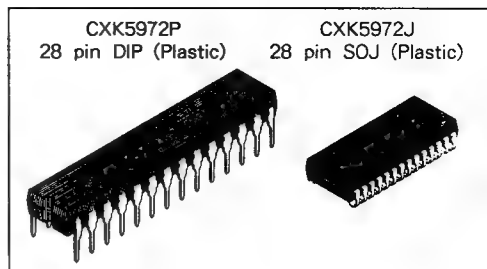
SOJ-28P-01

Description

The CXK5972P/J is a high speed CMOS static RAM which consists of 8,192-word × 9-bit. It operates at 15ns and 20ns high speed from 5V single power supply.

Features

- High speed, low power consumption :
Access time (Max.) Power consumption (Typ., Cycle=Min.)
CXK5972P/J-15 15ns 400mW
CXK5972P/J-20 20ns 325mW
- Single +5V power supply : 5V ± 10 %
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three state output.
- Directly TTL compatible all inputs and outputs.
- Available in 28 pin 300mil DIP, 300mil SOJ package.



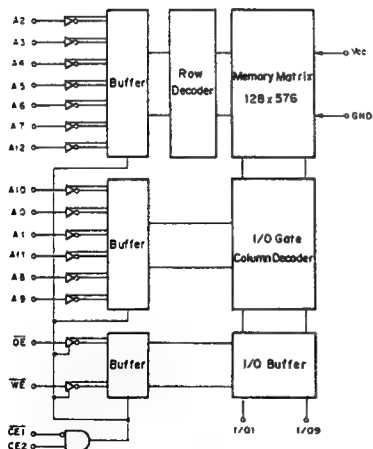
Function

8,192-word × 9-bit static RAM

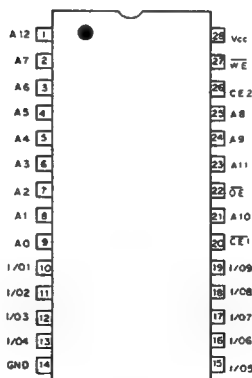
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O9	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O1 to I/O9	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10 %, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	-1	μA
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL}	-1	—	-1	μA
Operating power supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	—	—	
Average operating current	I _{CC2}	Cycle = Min, Duty = 100 %, I _{OUT} = 0mA	-15	—	80	mA
			-20	—	65	
Standby current	I _{SB1}	CE1 ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	1	mA
	I _{SB2}	CE1 = V _{IH} or CE2 = V _{IL} , V _{IN} = V _{IH} /V _{IL} , Cycle = Min.	—	15	25	
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	6	pF

Note) This parameter is sampled and is not 100% tested.

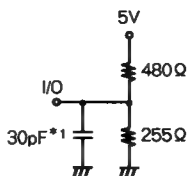
AC characteristics

• AC test conditions

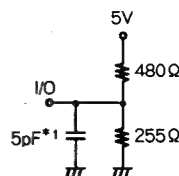
(V_{CC} = 5V ± 10 %, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	tr = 3ns
Input fall time	tf = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



*1. including scope and jig capacitance

*2. for tLZ1, tLZ2, tOLZ, tHZ1, tHZ2, tOHZ, tOW, tWHZ

Fig. 1

• Read cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	15	—	20	—	ns
Address access time	t _{AA}	—	15	—	20	ns
Chip enable access time ($\overline{\text{CE1}}$)	t _{CO1}	—	15	—	20	ns
Chip enable access time (CE2)	t _{CO2}	—	15	—	20	ns
Output enable to output valid	t _{OE}	—	8	—	10	ns
Output hold from address change	t _{OH}	5	—	5	—	ns
Chip enable to output in low Z ($\overline{\text{CE1}}$, CE2)	t _{LE1} *, t _{LE2} *	5	—	5	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ} *	2	—	2	—	ns
Chip disable to output in high Z ($\overline{\text{CE1}}$, CE2)	t _{HE1} *, t _{HE2} *	0	8	0	9	ns
Output disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	0	7	0	8	ns
Chip enable to power up time ($\overline{\text{CE1}}$, CE2)	t _{PU}	0	—	0	—	ns
Chip disable to power down time ($\overline{\text{CE1}}$, CE2)	t _{PD}	—	15	—	20	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

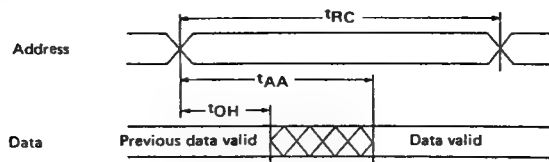
• Write cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	15	—	20	—	ns
Address valid to end of write	t _{AW}	12	—	14	—	ns
Chip enable to end of write	t _{CW}	12	—	14	—	ns
Data to write time overlap	t _{DW}	9	—	10	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	11	—	13	—	ns
Address set up time	t _{AS}	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	t _{WR}	0	—	0	—	ns
Write recovery time ($\overline{\text{CE1}}$, CE2)	t _{WR1}	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	7	0	9	ns

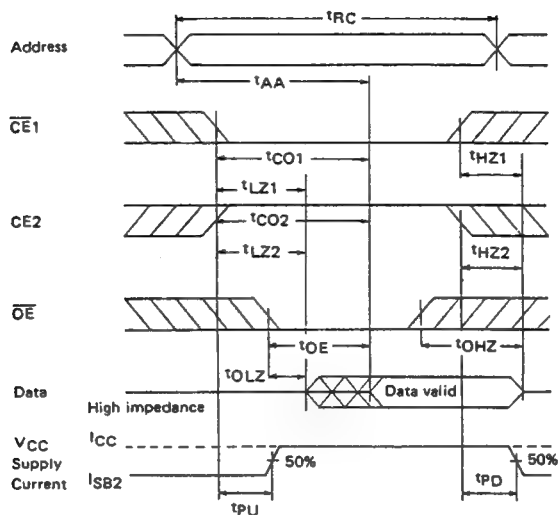
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

Timing Waveform

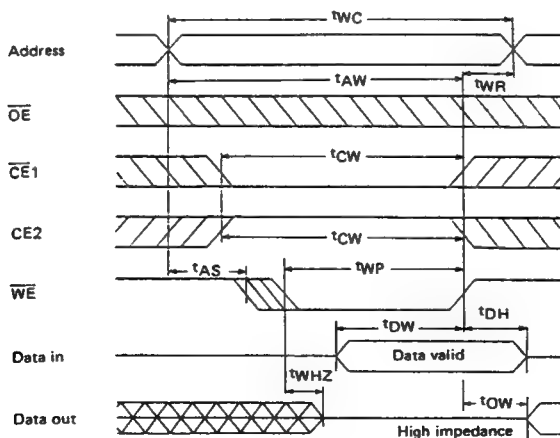
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



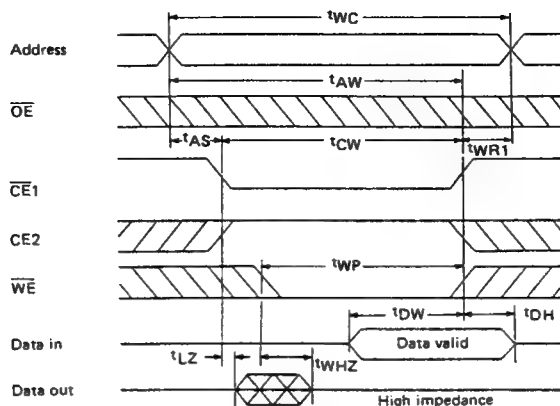
- Read cycle (2) : $\overline{WE} = V_{IH}$



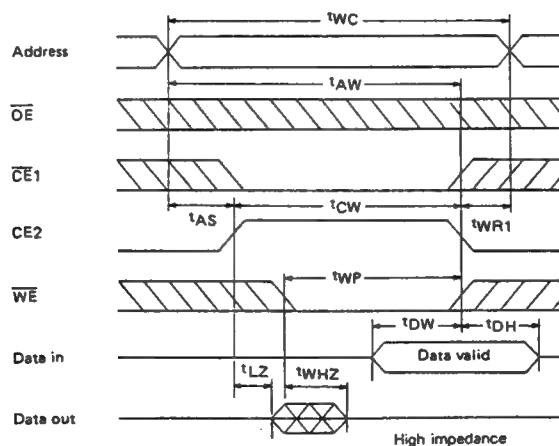
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : $\overline{CE2}$ control

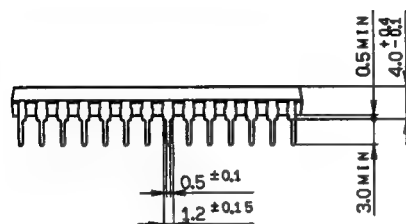
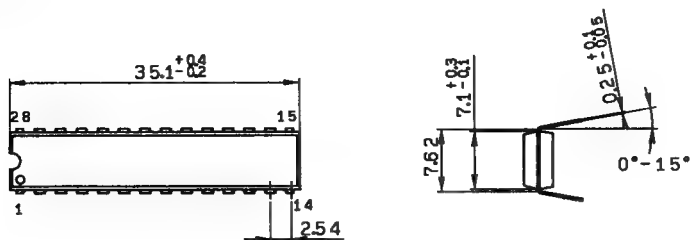


* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

CXK5972P

28pin DIP (Plastic) 300mil 2.0g

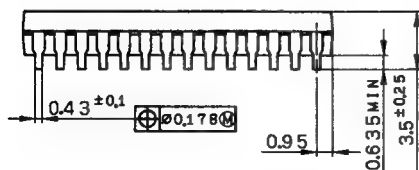
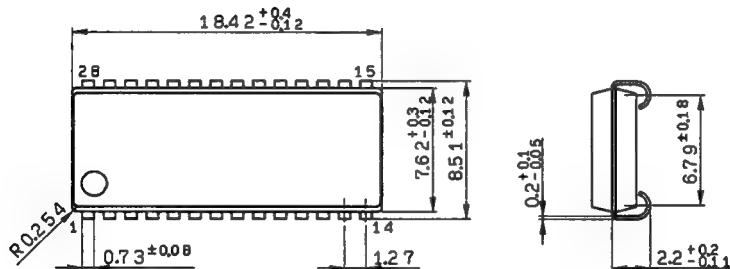


SONY NAME	DIP-28P-06
EIAJ NAME	*DIP028-P-0300-A
JEDEC CODE	MO-058-AB *

* (Similar)

CXK5972J

28pin SOJ (Plastic) 300mil 0.8g



SONY NAME	SOJ-28P-01
EIAJ NAME	*SOJ028-P-0300-A
JEDEC CODE	MO-077-AB

D 0.1

SONY. CXK58257AP/ASP/AM

32768-word × 8-bit High Speed CMOS Static RAM

Description

CXK58257AP/ASP/AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

* 300mil DIP covers only L-version.

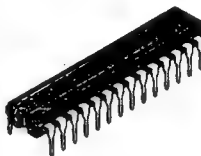
Features

- Fast access time : (Access time)
 CXK58257AP/ASP/AM-70L, 70LL 70ns(Max.)
 CXK58257AP/ASP/AM-85L, 85LL 85ns(Max.)
 CXK58257AP/ASP/AM-10L, 10LL 100ns(Max.)
 CXK58257AP/ASP/AM-12L, 12LL 120ns(Max.)
- Low power operation :
 CXK58257AP/AM-70LL, 85LL, 10LL, 12LL ;
 Standby : 1 μ W (Typ.)
 Operation : 15mW (Typ.)
 CXK58257AP/ASP/AM-70L, 85L, 10L, 12L ;
 Standby : 2.5 μ W (Typ.)
 Operation : 15mW (Typ.)
- Single +5V supply : +5V \pm 10 %
- Fully static memory...No clock or timing
 strobe required
- Equal access and cycle time
- Common data input and output :
 three state output
- Directly TTL compatible :
 All inputs and outputs



CXK58257ASP
28 pin DIP (Plastic)

CXK58257AM
28 pin SOP (Plastic)



- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

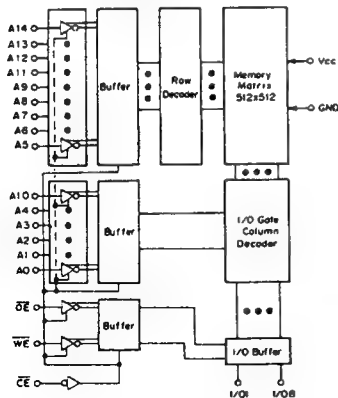
Function

32768-word X 8-bit static RAM

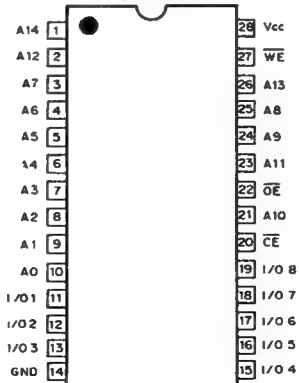
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O0 to I/O8	Data input/output
$\overline{\text{CE}}$	Chip enable input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{OE}}$	Output enable input
V _{cc}	+5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V _{CC}		− 0.5 to + 7.0	V
Input voltage	V _{IN}		− 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}		− 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK58257AP/ASP	1.0	W
		CXK58257AM	0.7	
Operating temperature	T _{opr}		0 to + 70	°C
Storage temperature	T _{stg}		− 55 to + 150	°C
Soldering temperature	T _{solder}		260 • 10	°C • sec

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.

Truth Table

CE	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	x	x	Not selected	High Z	I _{s81} , I _{s82}
L	H	H	Not selected	High Z	I _{cc1} , I _{cc2}
L	L	H	Read	Data out	I _{cc1} , I _{cc2}
L	x	L	Write	Data in	I _{cc1} , I _{cc2}

x : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions		-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}		-0.5	—	0.5	-0.5	—	0.5	μA
Output leakage current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ V _{I/O} = GND to V _{CC}		-0.5	—	0.5	-0.5	—	0.5	μA
Operating power supply current	I _{CC1}	$\overline{CE} = V_{IL}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA		—	3	10	—	3	10	mA
		$\overline{CE} \leq 0.2V$ V _{IN} $\leq 0.2V$ or $\geq V_{CC} - 0.2V$		—	1	5	—	1	5	
Average operating current	I _{CC2}	Cycle = Min, Duty = 100 %, I _{OUT} = 0mA	70L/70LL	—	30	50	—	30	50	mA
			85L/85LL	—	25	50	—	25	50	
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	0 to 70°C	—	—	25	—	—	5	μA
			0 to 40°C	—	—	5	—	—	1	
			25°C	—	0.5	2	—	0.2	0.5	
		I _{SB2}	$\overline{CE} = V_{IH}$	—	0.4	2	—	0.4	2	mA
Output high voltage	V _{OH}	I _{OH} = -1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	pF

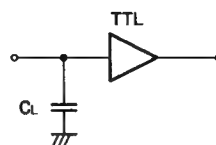
Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions

(V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item		Conditions
Input pulse high level		V _{IH} = 2.2V
Input pulse low level		V _{IL} = 0.8V
Input rise time		t _r = 5ns
Input fall time		t _f = 5ns
Input and output reference level		1.5V
Output load conditions	85L/85LL/10L/10LL/12L/12LL	C _L * = 100pF, 1TTL
	70L/70LL	C _L * = 30pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	-70L/70LL		-85L/85LL		-10L/10LL		-12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t _{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t _{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z (\overline{CE})	t _{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z (\overline{CE})	t _{HZ} *	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z (\overline{OE})	t _{OHZ} *	0	30	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

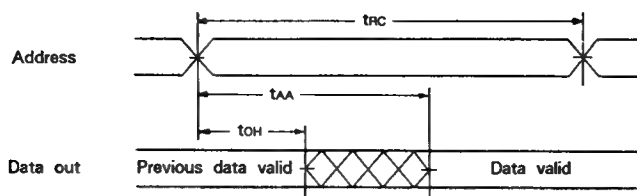
• Write cycle

Item	Symbol	-70L/70LL		-85L/85LL		-10L/10LL		-12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (\overline{CE})	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

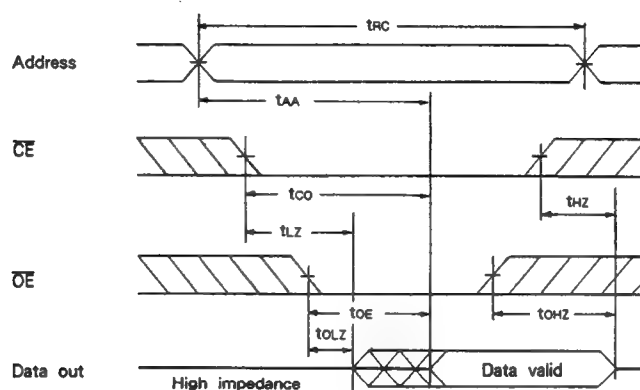
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

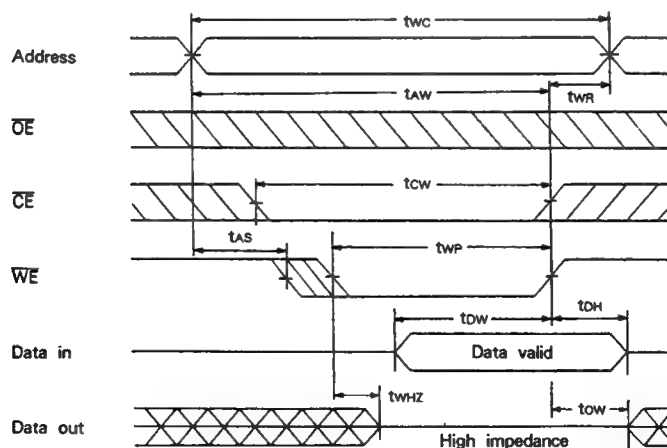
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



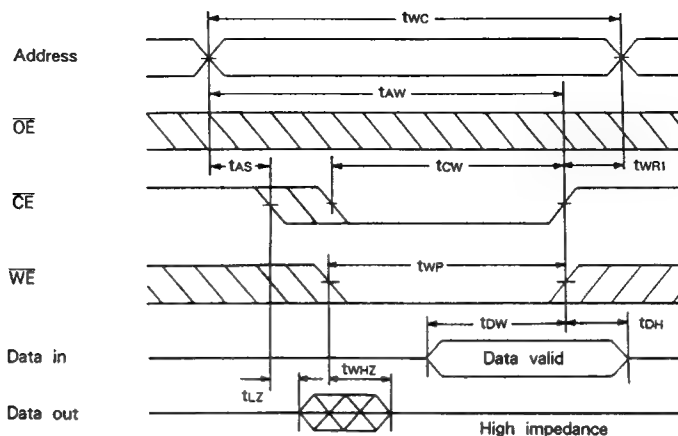
- Read cycle (2) : $\overline{WE} = V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE}}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

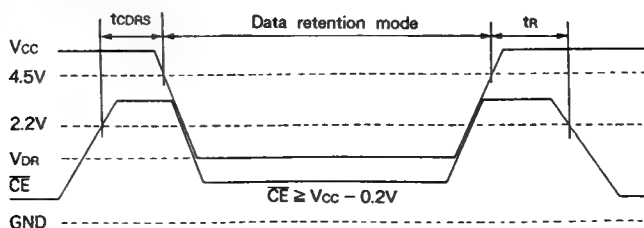
Data Retention Characteristics

($T_a = 0$ to 70°C)

Item	Symbol	Test conditions	-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}$	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0\text{V}$ $\overline{\text{CE}} \geq 2.8\text{V}$	$T_a = 0$ to 70°C			—	—	3	μA
			$T_a = 0$ to 40°C			—	—	0.6	
			25°C			—	0.25	1	
	I_{CCDR2}	$V_{CC} = 2.0$ to 5.5V $\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}$	—	0.5	25	—	0.2	5	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t_R		t_{RC}^*	—	—	t_{RC}^*	—	—	ns

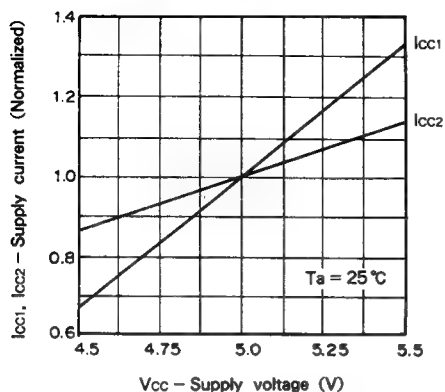
* t_{RC} : Read cycle time

Data retention waveform

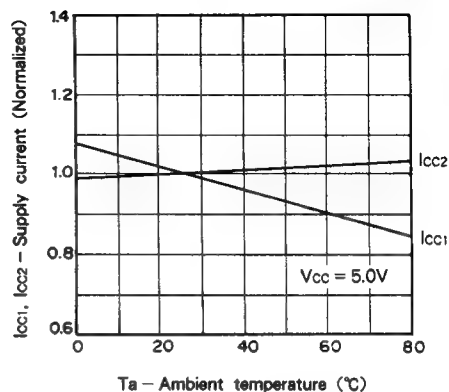


Example of Representative Characteristics

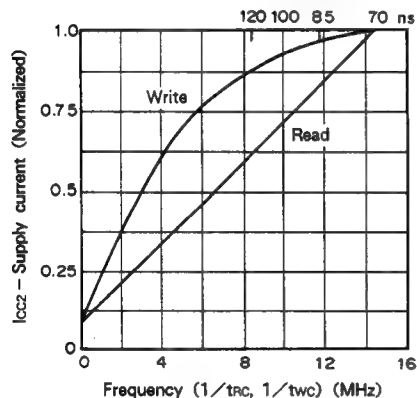
Supply current vs. Supply voltage



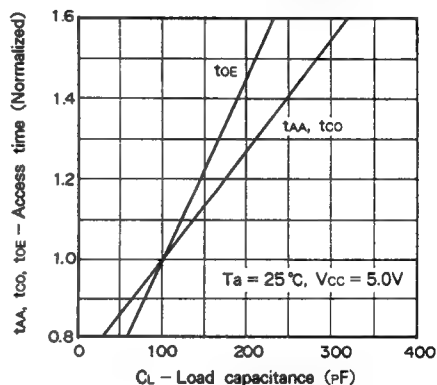
Supply current vs. Ambient temperature



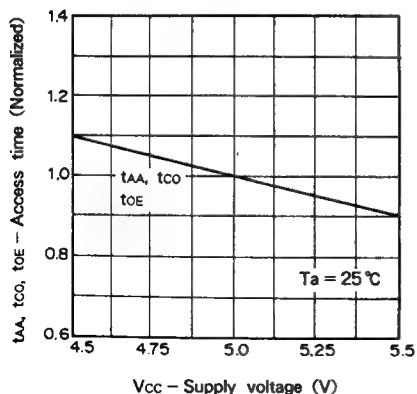
Supply current vs. Frequency



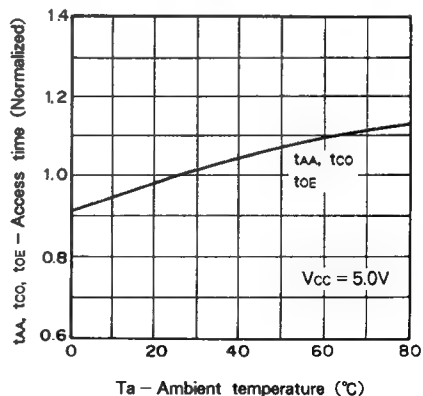
Access time vs. Load capacitance



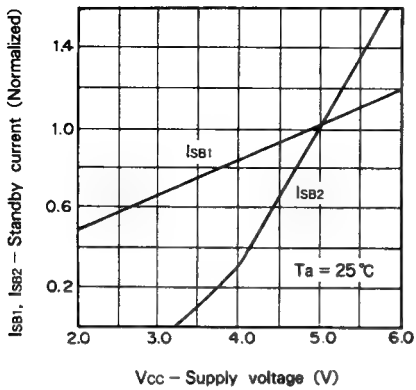
Access time vs. Supply voltage



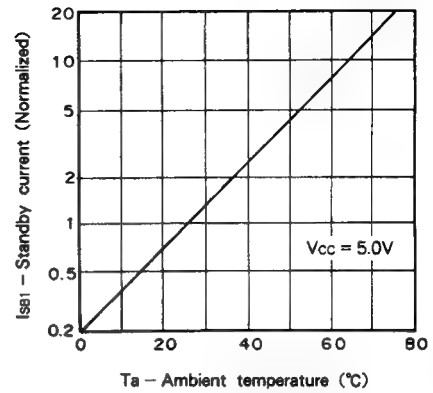
Access time vs. Ambient temperature



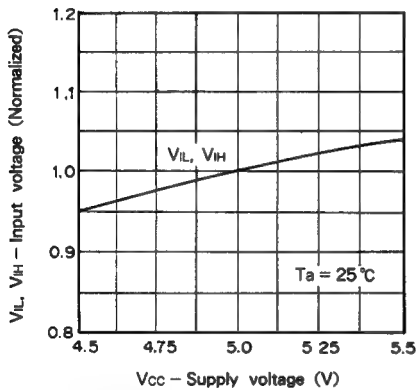
Standby current vs. Supply voltage



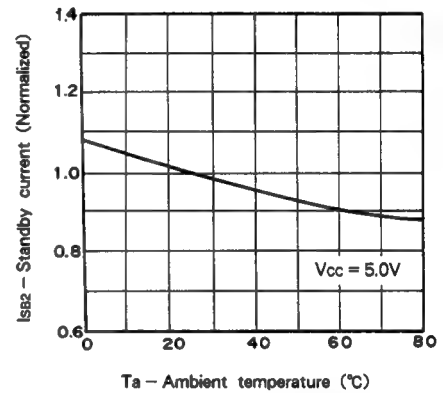
Standby current vs. Ambient temperature



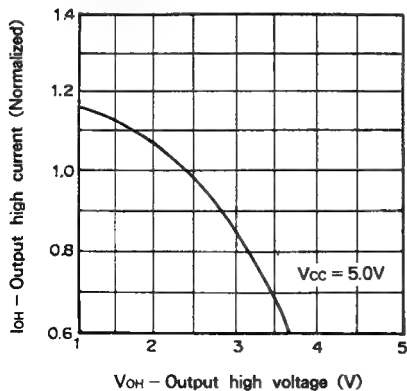
Input voltage level vs. Supply voltage



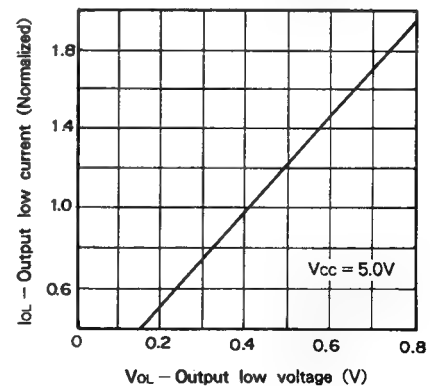
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



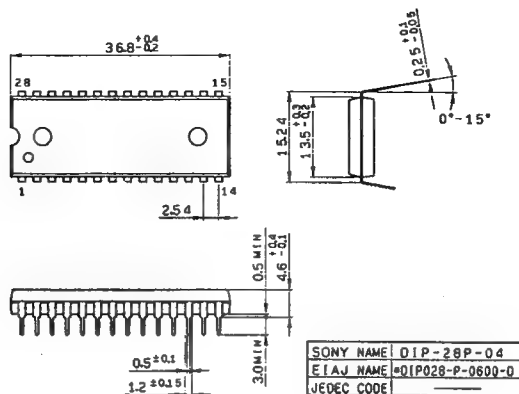
Output low current vs. Output low voltage



Package Outline Unit : mm

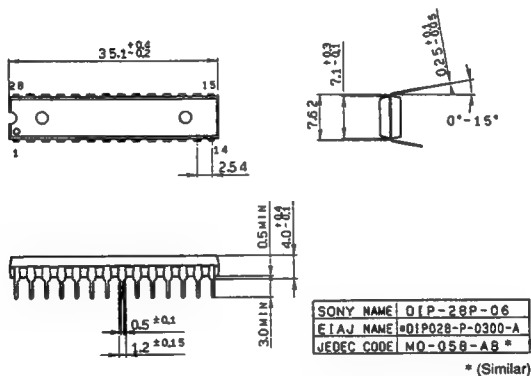
CXK58257AP

28pin DIP (Plastic) 600mil 4.2g



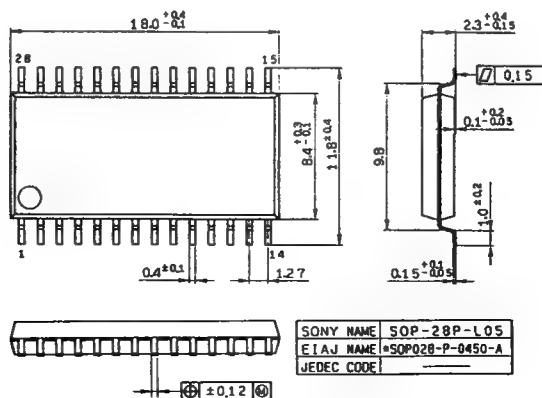
CXK58257ASP

28pin DIP (Plastic) 300mil 2.0g



CXK58257AM

28pin SOP (Plastic) 450mil 0.7g



32768-word × 8-bit High Speed CMOS Static RAM

Description

CXK58257ATM/AYM is a 256K bits, 32,768 words by 8 bits, CMOS static RAM.

It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current.

Features

- Thin Small-outline package :
CXK58257ATM : 8mm×13.4mm 28 pin TSOP
CXK58257AYM : 8mm×13.4mm 28 pin TSOP
(Mirror image pinout)
- Low stand-by current :
L-Version :
25 μ A (Max.) @ $V_{CC} = 5.5V$, $T_a = 0$ to $70^\circ C$
LL-Version :
5 μ A (Max.) @ $V_{CC} = 5.5V$, $T_a = 0$ to $70^\circ C$
- Low voltage data retention : 2.0V (Min.)
- Fast access time : (Access time)
CXK58257ATM/AYM-70L, -70LL 70ns (Max.)
CXK58257ATM/AYM-85L, -85LL 85ns (Max.)
CXK58257ATM/AYM-10L, -10LL 100ns (Max.)
CXK58257ATM/AYM-12L, -12LL 120ns (Max.)
- Single +5V Supply : $5V \pm 10\%$

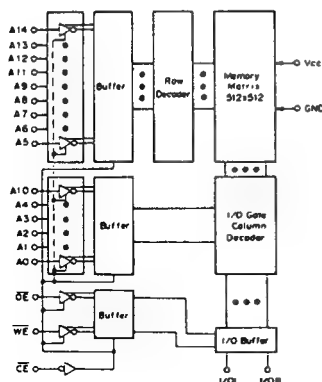
Function

32768-word × 8-bit static RAM

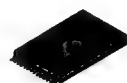
Structure

Silicon gate CMOS IC

Block Diagram



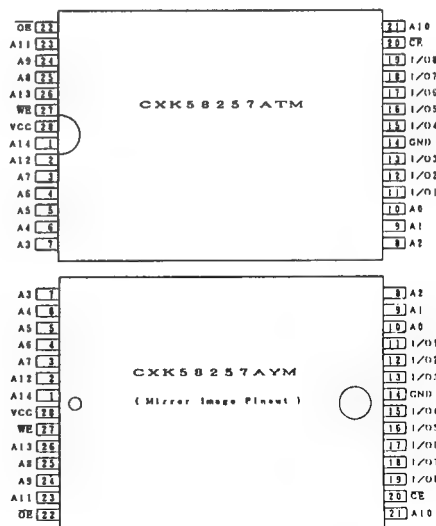
CXK58257ATM 28 pin TSOP (Plastic) CXK58257AYM 28 pin TSOP (Plastic)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O0 to I/O8	Data input/output
\overline{CE}	Chip enable input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
V_{CC}	+5V power supply
GND	Ground

Pin Configuration (Top View)



Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to + 7.0	V
Input voltage	V _{IH}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature	T _{solder}	235 ± 10	°C · sec

* V_{IH}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Not selected	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions		- 70L/85L/10L/12L			- 70LL/85LL/10LL/12LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}		- 0.5	—	0.5	- 0.5	—	0.5	μA
Output leakage current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ V _{I/O} = GND to V _{CC}		- 0.5	—	0.5	- 0.5	—	0.5	μA
Operating power supply current	I _{CC1}	$\overline{CE} = V_{IL}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA		—	3	10	—	3	10	mA
		$\overline{CE} \leq 0.2V$ V _{IN} $\leq 0.2V$ or $\geq V_{CC} - 0.2V$		—	1	5	—	1	5	
Average operating current	I _{CC2}	Cycle = Min, Duty = 100 %, I _{OUT} = 0mA	70L/70LL	—	30	50	—	30	50	mA
			85L/85LL	—	25	50	—	25	50	
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	0 to 70°C	—	—	25	—	—	5	μA
			0 to 40°C	—	—	5	—	—	1	
			25°C	—	0.5	2	—	0.2	0.5	
	I _{SB2}	$\overline{CE} = V_{IH}$	—	0.4	2	—	0.4	2	mA	
Output high voltage	V _{OH}	I _{OH} = - 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	pF

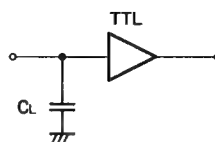
Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions

(V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Conditions	
Input pulse high level	V _{IH} = 2.2V	
Input pulse low level	V _{IL} = 0.8V	
Input rise time	tr = 5ns	
Input fall time	tf = 5ns	
Input and output reference level	1.5V	
Output load conditions	85L/85LL/10L/10LL/12L/12LL	C _L * = 100pF, 1TTL
	70L/70LL	C _L * = 30pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	-70L/70LL		-85L/85LL		-10L/10LL		-12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t _{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t _{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z (CE)	t _{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z (OE)	t _{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z (CE)	t _{HZ} *	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z (OE)	t _{OHZ} *	0	30	0	30	0	35	0	40	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

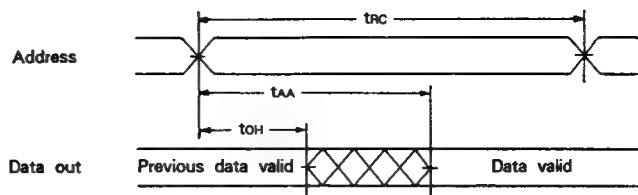
• Write cycle

Item	Symbol	-70L/70LL		-85L/85LL		-10L/10LL		-12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (CE)	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

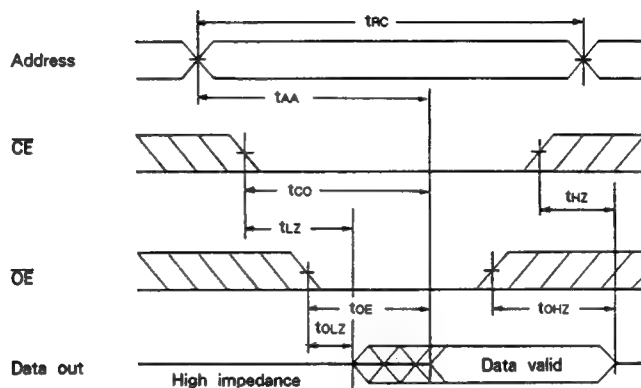
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

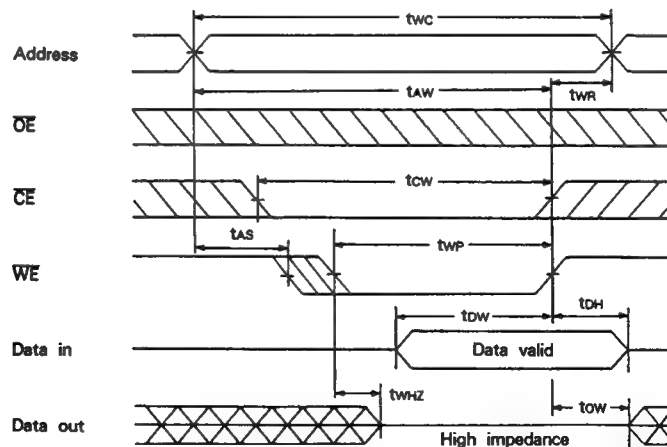
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



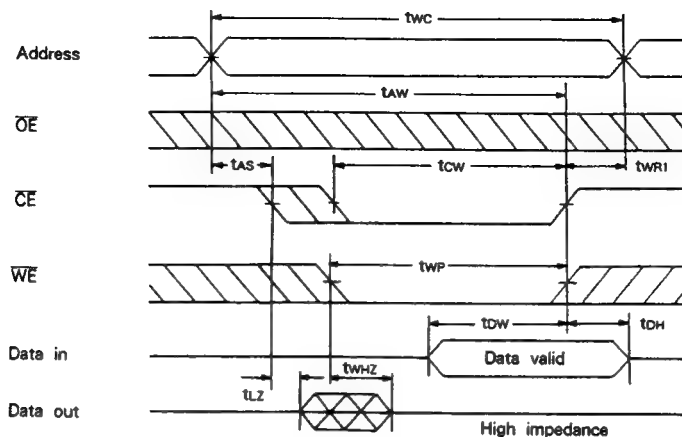
- Read cycle (2) : $\overline{WE} = V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE}}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

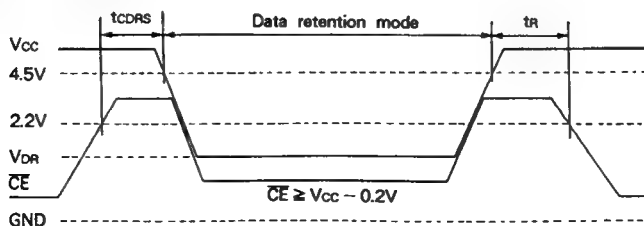
Data Retention Characteristics

($T_a = 0$ to 70°C)

Item	Symbol	Test conditions		-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	$\overline{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}$		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	$V_{\text{CC}} = 3.0\text{V}$ $\overline{\text{CE}} \geq 2.8\text{V}$	T _a = 0 to 70°C	—	—	10	—	—	3	μA
			T _a = 0 to 40°C	—	—	2	—	—	0.6	
			25°C	—	0.25	1	—	0.1	0.3	
	I _{CCDR2}	$V_{\text{CC}} = 2.0$ to 5.5V $\overline{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}$	—	0.5	25	—	0.2	5	μA	
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t _R			t _{RC} *	—	—	t _{RC} *	—	—	ns

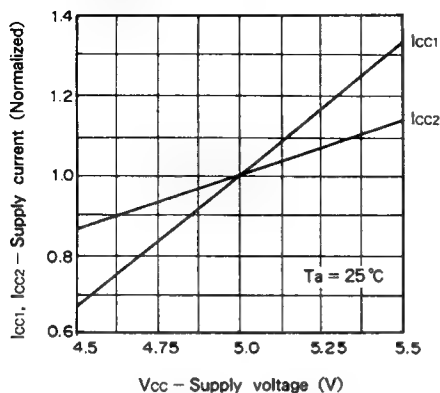
* t_{RC} : Read cycle time

Data retention waveform

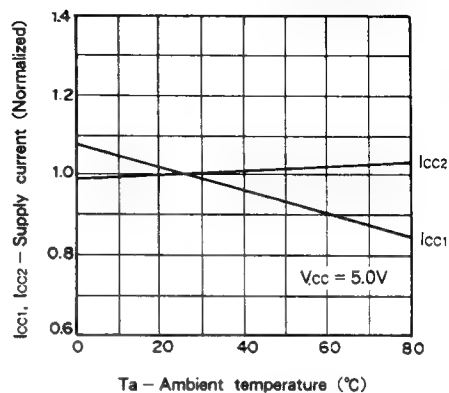


Example of Representative Characteristics

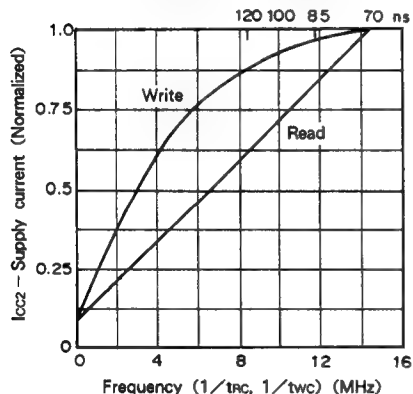
Supply current vs. Supply voltage



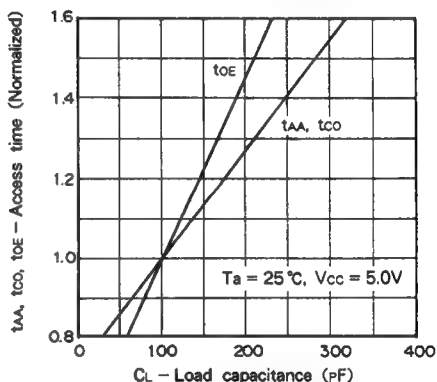
Supply current vs. Ambient temperature



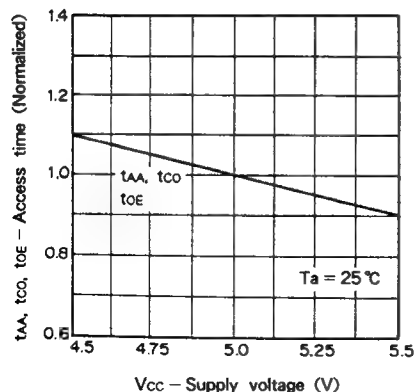
Supply current vs. Frequency



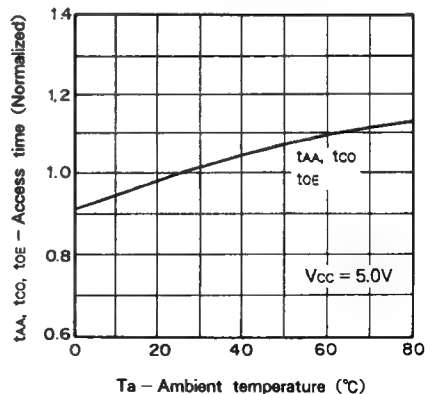
Access time vs. Load capacitance



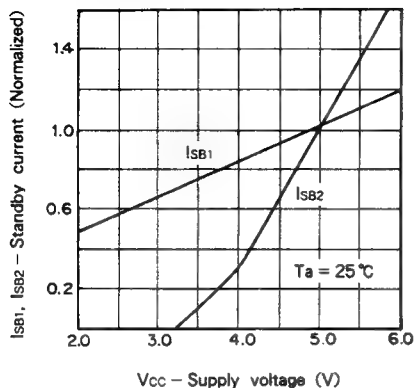
Access time vs. Supply voltage



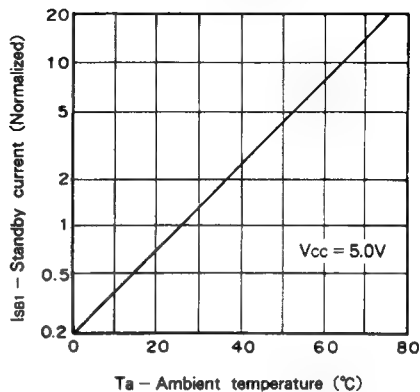
Access time vs. Ambient temperature



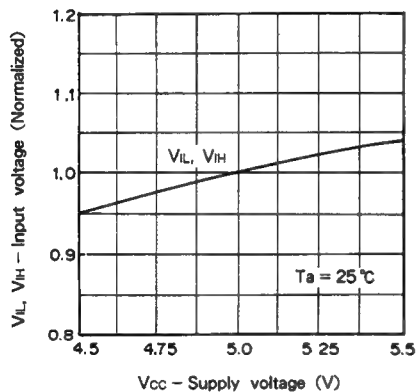
Standby current vs. Supply voltage



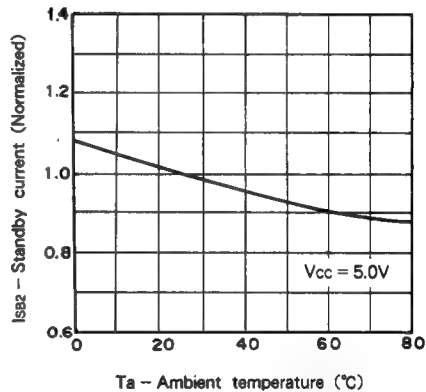
Standby current vs. Ambient temperature



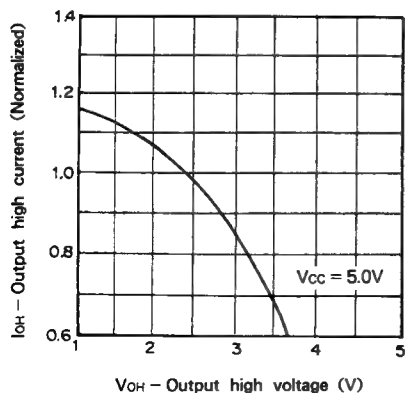
Input voltage level vs. Supply voltage



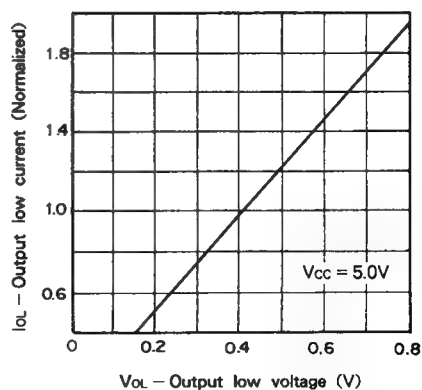
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



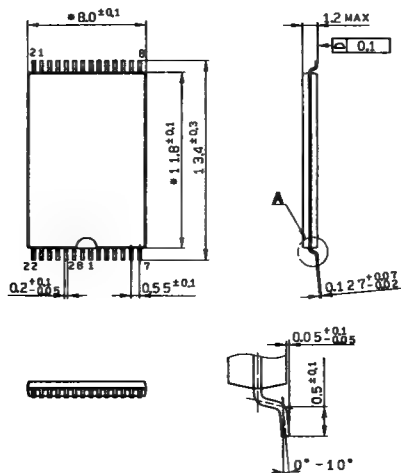
Output low current vs. Output low voltage



Package Outline Unit : mm

CXK58257ATM

28pin TSOP (Plastic)



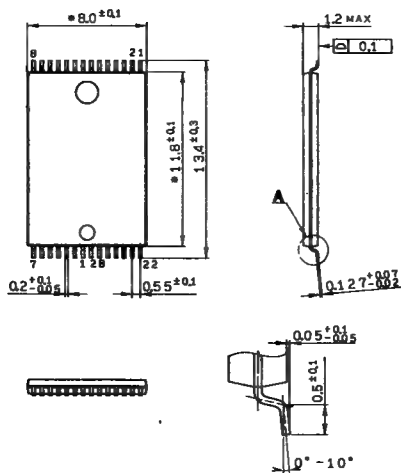
Detailed drawing of A

SONY NAME	TSOP-28P-L01
EIAJ NAME	TSOP028-P-0000-A
JEDEC CODE	

Notes: Dimensions marked with *
do not include resin protrusion.

CXK58257AYM

28pin TSOP (Plastic)



Detailed drawing of A

SONY NAME	TSOP-28P-L01R
EIAJ NAME	TSOP028-P-0000-B
JEDEC CODE	

Notes: Dimensions marked with *
do not include resin protrusion.

SONY CXK58257AP/AM -70LX/85LX/10LX/12LX -70LLX/85LLX/10LLX/12LLX*

32768-word × 8-bit High Speed CMOS Static RAM

Description

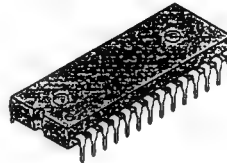
CXK58257AP/AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

* DIP covers only LX-version.

Features

- Extended operating temperature range: -25 to 85 °C
- Fast access time: (Access time)
CXK58257AP/AM-70LX,70LLX 70ns (Max.)
CXK58257AP/AM-85LX,85LLX 85ns (Max.)
CXK58257AP/AM-10LX,10LLX 100ns (Max.)
CXK58257AP/AM-12LX,12LLX 120ns (Max.)
- Low power operation:
CXK58257AM-70LLX, 85LLX,10LLX,12LLX;
Standby : 1 µW (Typ.)
Operation : 15mW (Typ.)
CXK58257AP/AM-70LX, 85LX,10LX,12LX;
Standby : 2.5 µW (Typ.)
Operation : 15mW (Typ.)
- Single +5V supply: +5V ± 10%
- Fully static memory...No clock or timing strobe required
- Equal access and cycle time

CXK58257AP
28 pin DIP (Plastic)



CXK58257AM
28 pin SOP (Plastic)



- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin 600mil DIP and 450mil SOP

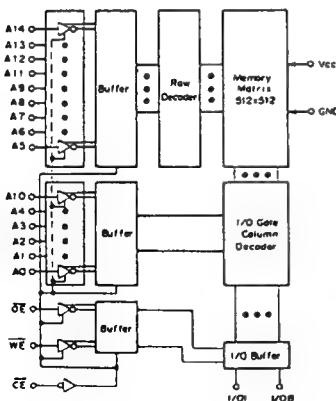
Function

32768-word × 8-bit static RAM

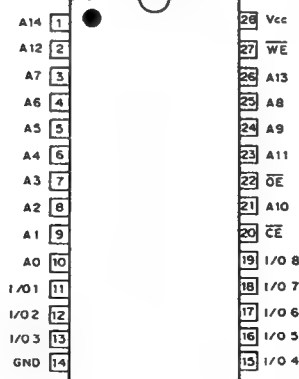
Structure

Silicon gate CMOS IC

Block diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A ₀ to A ₁₄	Address input
I/O ₁ to I/O ₈	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	− 0.5 to +7.0	V
Input voltage	V _{IH}	− 0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{IO}	− 0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK58257AP 1.0	W
		CXK58257AM 0.7	
Operating temperature	T _{opr}	− 25 to +85	°C
Storage temperature	T _{stg}	− 55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{IO} = − 3.0V Min. for pulse width less than 50ns.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O8	V _{CC} Current
H	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Not selected	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	x	L	Write	Data in	I _{CC1} , I _{CC2}

x : "H" or "L"

DC Recommended Operating Conditions (Ta= − 25 to +85°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	− 0.3 *	—	0.8	V

* V_{IL} = − 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a= - 25 to +85 °C)

Item	Symbol	Test conditions		-70LX/85LX/10LX/12LX			-70LLX/85LLX/10LLX/12LLX			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		- 0.5	—	0.5	- 0.5	—	0.5	μA
Output leakage current	I _{LO}	\overline{CE} =V _{IH} or \overline{OE} =V _{IH} V _{I/O} =GND to V _{CC}		- 0.5	—	0.5	- 0.5	—	0.5	μA
Operating power supply current	I _{CC1}	\overline{CE} =V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA		—	3	10	—	3	10	mA
		$\overline{CE} \leq 0.2V$ V _{IN} $\leq 0.2V$ or $\geq V_{CC}-0.2V$		—	1	5	—	1	5	
Average operating current	I _{CC2}	Cycle=Min, Duty=100% I _{OUT} =0mA	70LX/70LLX	—	30	60	—	30	60	mA
			85LX/85LLX	—	25	60	—	25	60	
			10LX/10LLX	—	23	60	—	23	60	
			12LX/12LLX	—	20	60	—	20	60	
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$	-25 to 85 °C	—	—	50	—	—	10	μA
			-25 to 70 °C	—	—	25	—	—	5	
			-25 to 40 °C	—	—	5	—	—	1	
			25 °C	—	0.5	2	—	0.2	0.5	
	I _{SB2}	\overline{CE} =V _{IH}	—	0.4	2	—	0.4	2	mA	
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

(T_a=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

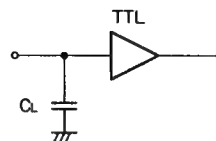
Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions

(V_{CC}=5V ± 10%, T_a=-25 to +85°C)

Item		Conditions
Input pulse high level		V _{IH} =2.4V
Input pulse low level		V _{IL} =0.6V
Input rise time		t _r =5ns
Input fall time		t _f =5ns
Input and output reference level		1.5V
Output load conditions	85LX/85LLX/10LX/ 10LLX/12LX/12LLX/	C _L * =100pF, 1TTL
	70LX/70LLX	C _L * =30pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t _{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t _{OH}	5	—	10	—	10	—	10	—	ns
Chip enable to output in low Z (\overline{CE})	t _{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z (\overline{CE})	t _{HZ} *	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z (\overline{OE})	t _{OHZ} *	0	30	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

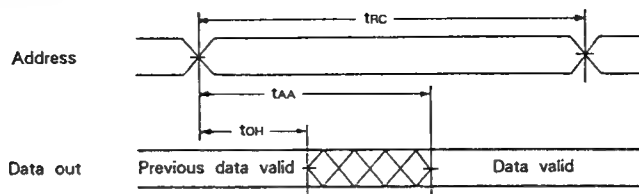
• Write cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	5	—	5	—	5	—	5	—	ns
Write recovery time (\overline{CE})	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

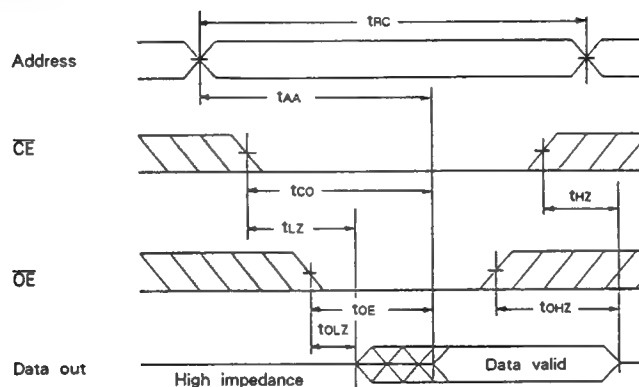
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

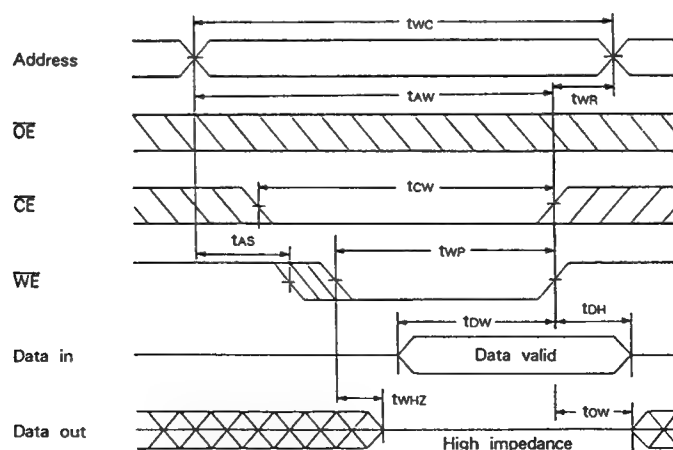
- Read cycle (1) : $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



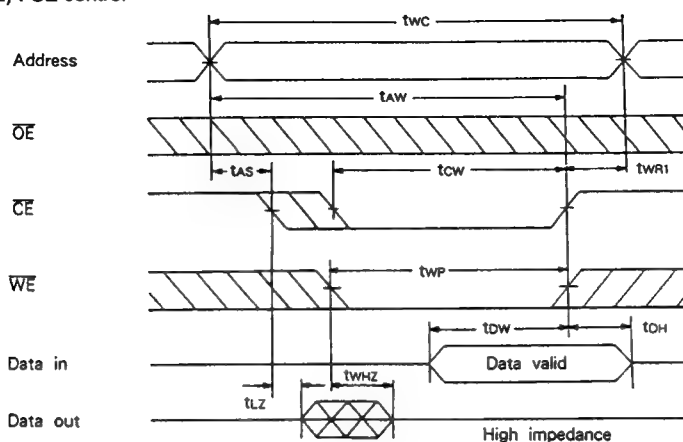
- Read cycle (2) : $\overline{WE}=V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE}}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

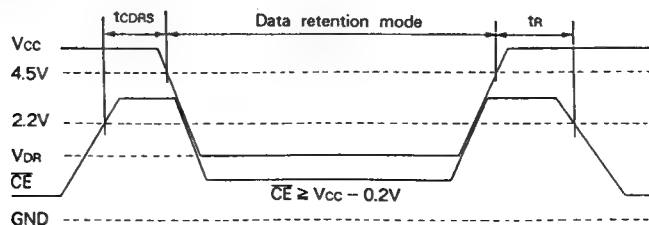
($T_a = -25$ to 85°C)

Item	Symbol	Test conditions	-70LX/85LX/10LX/12LX			-70LLX/85LLX/10LLX/12LLX			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}$	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0\text{V}$ $\overline{\text{CE}} \geq 2.8\text{V}$	-25 to 85°C	—	20	—	—	6	μA
			-25 to 70°C	—	10	—	—	3	
			-25 to 40°C	—	2	—	—	0.6	
			25°C	—	0.25	—	0.1	0.3	
	I_{CCDR2}	$V_{CC} = 2.0$ to 5.5V $\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}$	—	0.5 **	50	—	0.2 **	10	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t_R		$t_{RC} *$	—	—	$t_{RC} *$	—	—	ns

* t_{RC} : Read cycle time

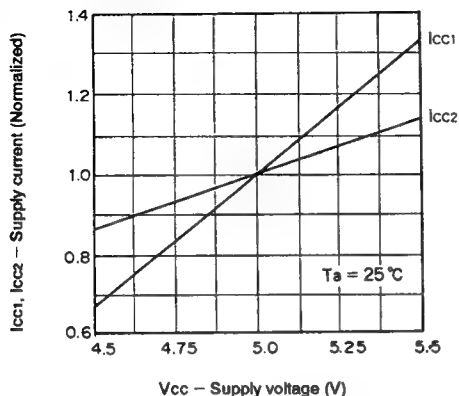
** $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

Data retention waveform

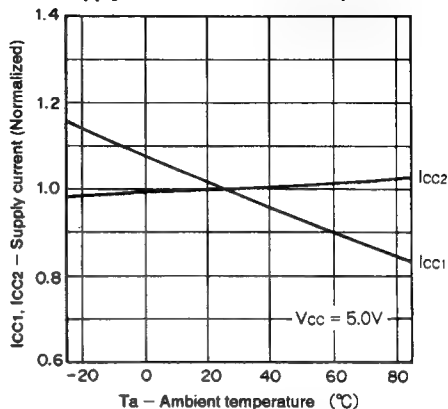


Example of Representative Characteristics

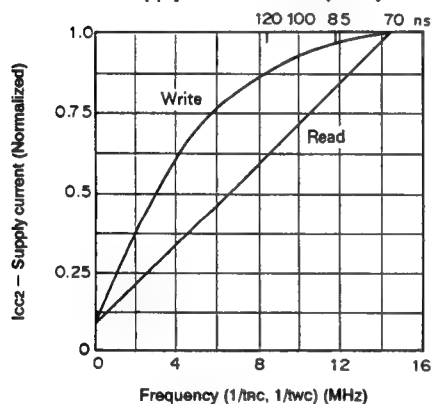
Supply current vs. Supply voltage



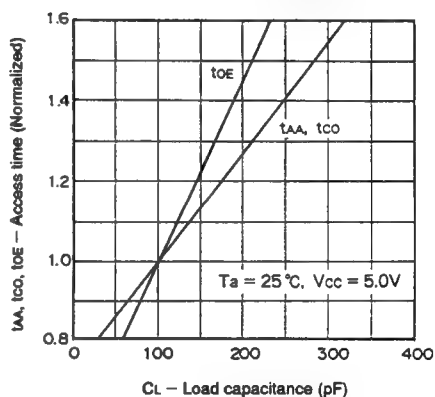
Supply current vs. Ambient temperature



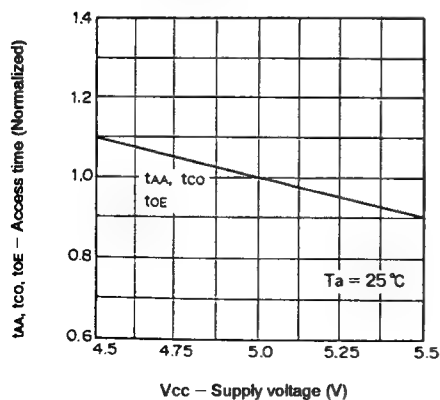
Supply current vs. Frequency



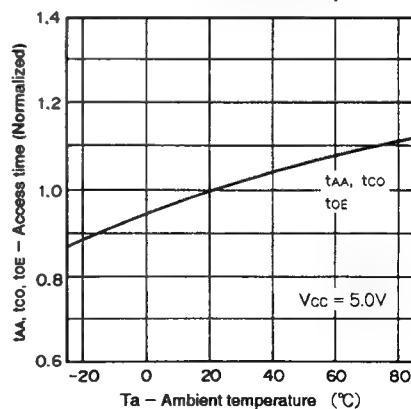
Access time vs. Load capacitance



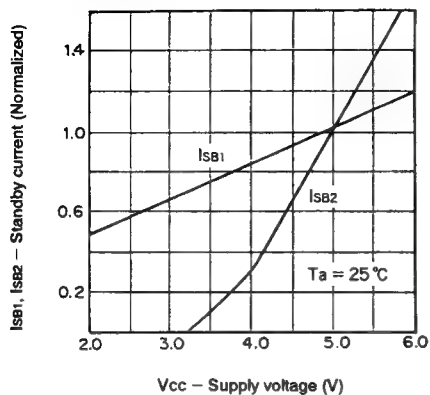
Access time vs. Supply voltage



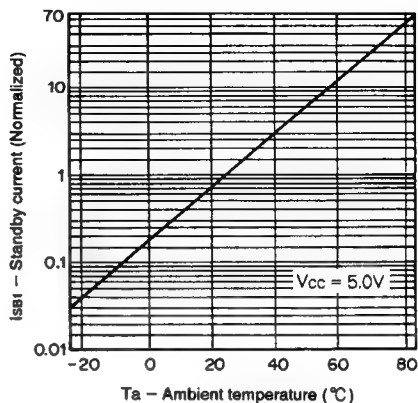
Access time vs. Ambient temperature



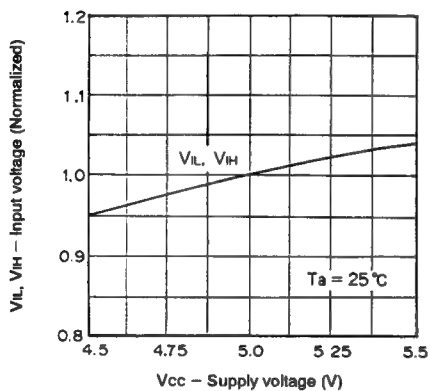
Standby current vs. Supply voltage



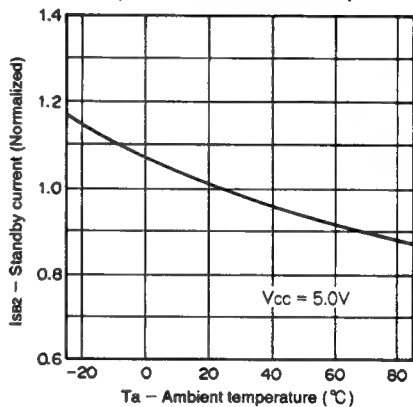
Standby current vs. Ambient temperature



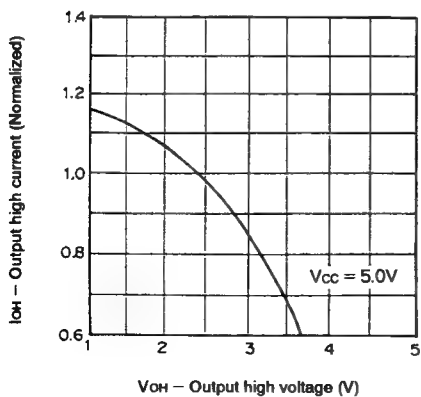
Input voltage level vs. Supply voltage



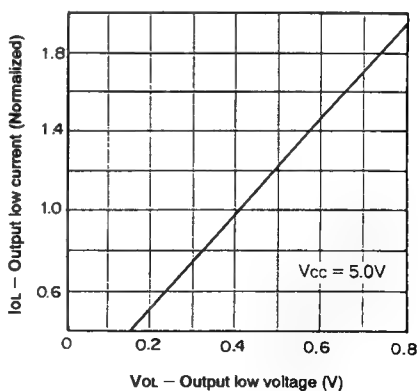
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



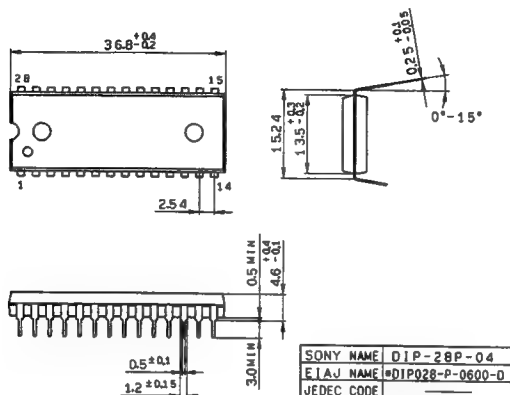
Output low current vs. Output low voltage



Package Outline Unit : mm

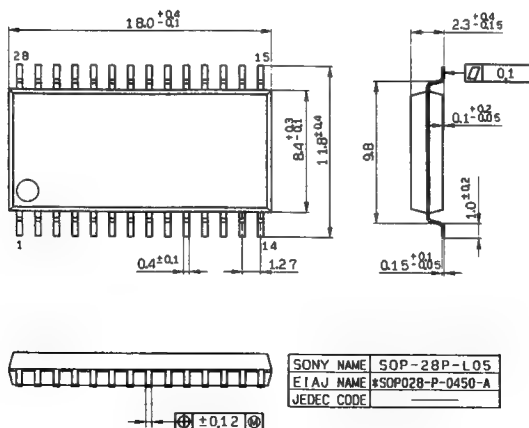
CXK58257AP

28pin DIP (Plastic) 600mil 4.2g



CXK58257AM

28pin SOP (Plastic) 450mil



SONY CXK58257ATM/AYM -70LLX/85LLX/10LLX/12LLX

32768-word × 8-bit High Speed CMOS Static RAM

Description

CXK58257ATM/AYM is a 256K bits, 32,768 words by 8 bits, CMOS static RAM.

It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current.

Features

- Extended operation temperature range: -25 to +85 °C
- Thin small-outline package:
CXK58257ATM: 8mm × 13.4mm 28 pin TSOP
CXK58257AYM: 8mm × 13.4mm 28 pin TSOP (Mirror image pinout)
- Low stand-by current:
10 μA (Max.) @Vcc=5.5V, Ta=-25 to +85 °C
- Low voltage data retention: 2.0V (Min.)
- Fast access time: (Access time)
CXK58257ATM/AYM-70LLX 70ns (Max.)
CXK58257ATM/AYM-85LLX 85ns (Max.)
CXK58257ATM/AYM-10LLX 100ns (Max.)
CXK58257ATM/AYM-12LLX 120ns (Max.)
- Single +5V Supply: 5V ± 10%

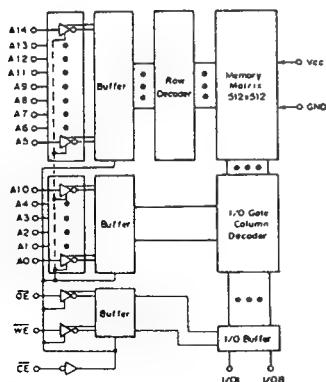
Function

32768-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

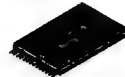
Block Diagram



CXK58257ATM
28 pin TSOP (Plastic)



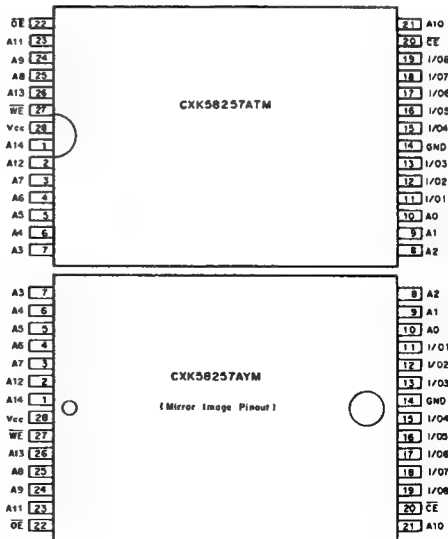
CXK58257AYM
28 pin TSOP (Plastic)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground

Pin Configuration (Top View)



Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	-25 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	235 • 10	°C • sec

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.**Truth Table**

CE	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Not selected	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta=-25 to +85°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics (Vcc=5V ± 10%, GND=0V, Ta=-25 to +85 °C)

Item	Symbol	Test conditions	-70LLX/85LLX/10LLX/12LLX			Unit
			Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	-0.5	—	0.5	μA
Output leakage current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ V _{I/O} =GND to V _{CC}	-0.5	—	0.5	μA
Operating power supply current	I _{CC1}	$\overline{CE}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	—	3	10	mA
		$\overline{CE} \leq 0.2V$ V _{IN} ≤ 0.2V or ≥ V _{CC} -0.2V	—	1	5	
Average operating current	I _{CC2}	Cycle=Min, Duty=100% I _{OUT} =0mA	70LLX	—	30	mA
			85LLX	—	25	
			10LLX	—	23	
			12LLX	—	20	
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$	-25 to +85 °C	—	—	μA
			-25 to +70 °C	—	—	
			-25 to +40 °C	—	—	
			+25 °C	—	0.2	
	I _{SB2}	$\overline{CE}=V_{IH}$	—	0.4	2	mA
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	V

* Vcc=5V, Ta=25 °C

I/O Capacitance

(Ta=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

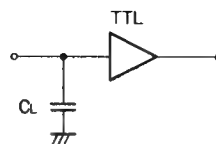
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

● AC test conditions

(V_{CC}=5V ± 10%, T_a=-25 to +85°C)

Item		Conditions
Input pulse high level		V _{IH} =2.4V
Input pulse low level		V _{IL} =0.6V
Input rise time		t _r =5ns
Input fall time		t _f =5ns
Input and output reference level		1.5V
Output load conditions	85LLX/10LLX/12LLX	C _L * =100pF, 1TTL
	70LLX	C _L * =30pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	- 70LLX		- 85LLX		- 10LLX		- 12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t _{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t _{OH}	5	—	10	—	10	—	10	—	ns
Chip enable to output in low Z (\overline{CE})	t _{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z (\overline{CE})	t _{HZ} *	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z (\overline{OE})	t _{OHZ} *	0	30	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

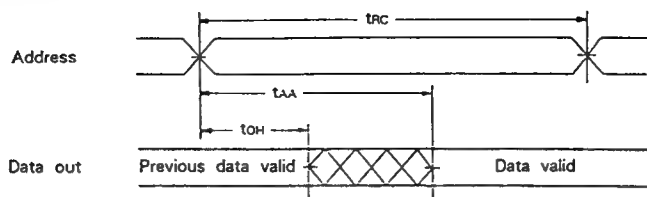
• Write cycle

Item	Symbol	- 70LLX		- 85LLX		- 10LLX		- 12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	5	—	5	—	5	—	5	—	ns
Write recovery time (\overline{CE})	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

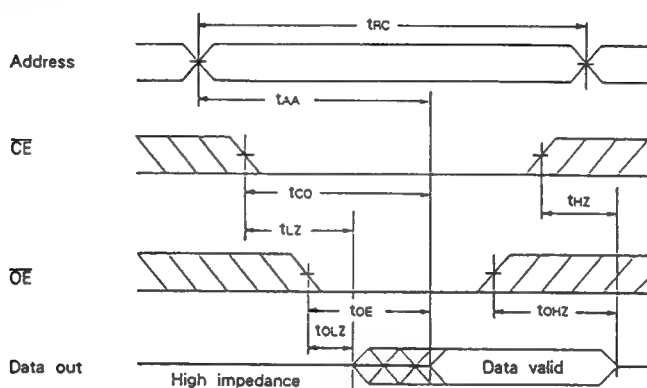
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

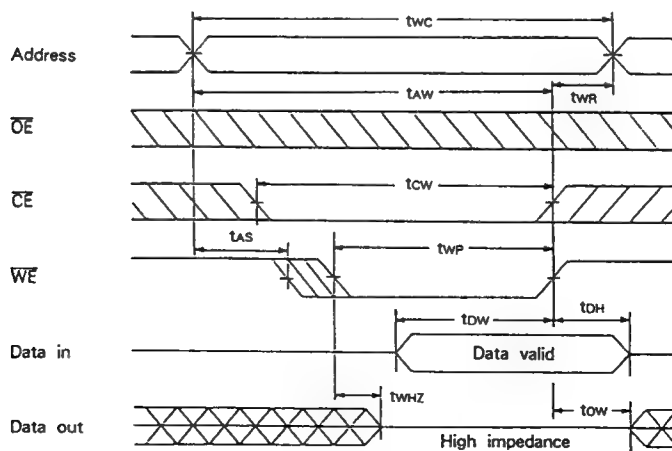
- Read cycle (1) : $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



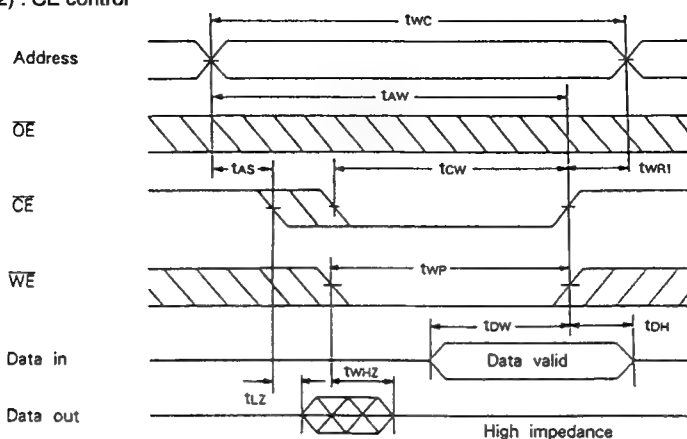
- Read cycle (2) : $\overline{WE}=V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2) : \overline{CE} control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

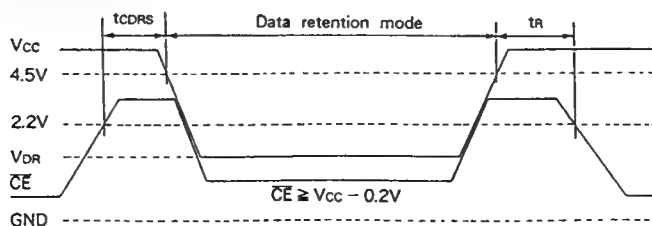
($T_a = -25$ to $+85^\circ\text{C}$)

Item	Symbol	Test conditions	-70LLX/85LLX/10LLX/12LLX			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$ $\overline{CE} \geq 2.8V$	-25 to $+85^\circ\text{C}$	—	6	μA
			-25 to $+70^\circ\text{C}$	—	3	
			-25 to $+40^\circ\text{C}$	—	0.6	
			$+25^\circ\text{C}$	—	0.1	
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V$ $\overline{CE} \geq V_{CC} - 0.2V$	—	0.2 **	10	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		$t_{RC} *$	—	—	ns

* t_{RC} : Read cycle time

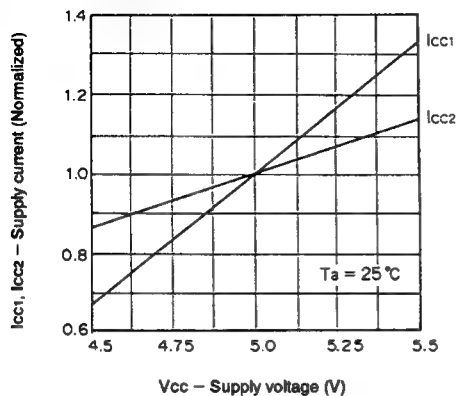
** $V_{CC} = 5V$, $T_a = 25^\circ\text{C}$

Data Retention Waveform

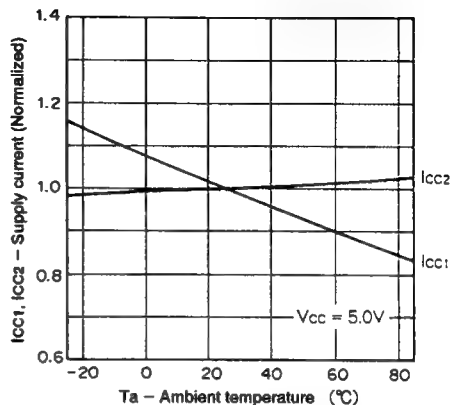


Example of Representative Characteristics

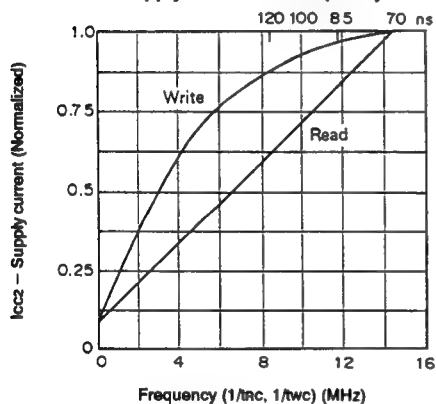
Supply current vs. Supply voltage



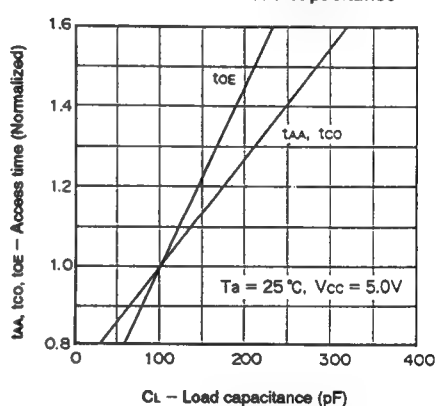
Supply current vs. Ambient temperature



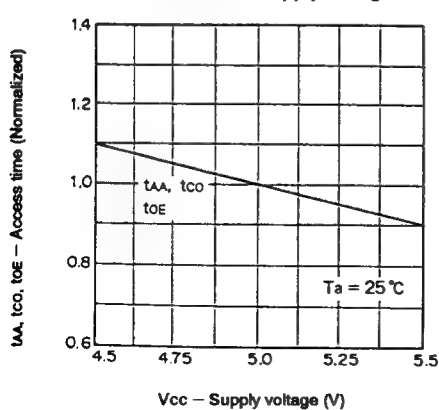
Supply current vs. Frequency



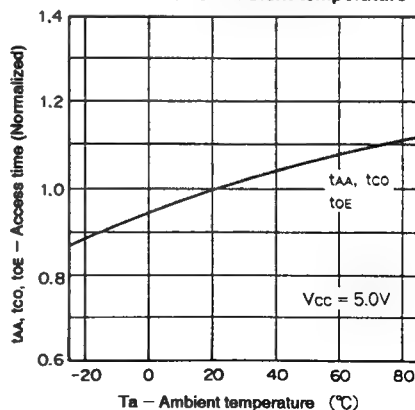
Access time vs. Load capacitance



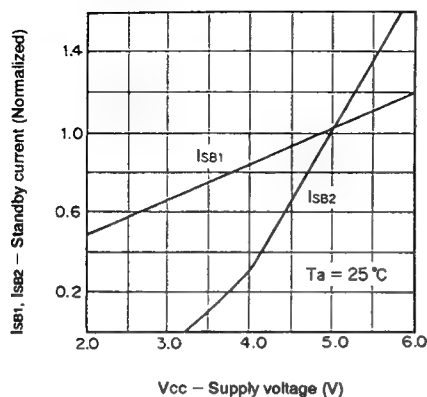
Access time vs. Supply voltage



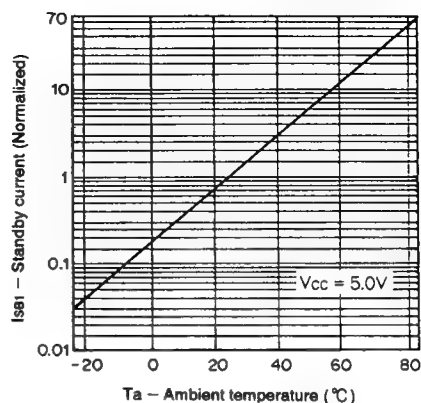
Access time vs. Ambient temperature



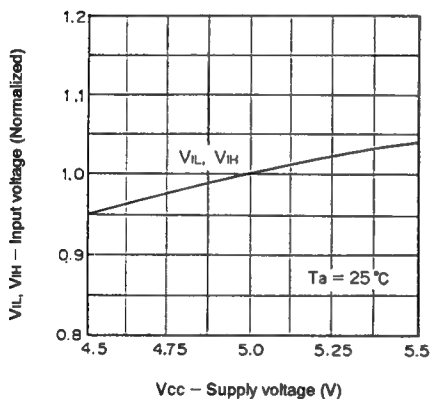
Standby current vs. Supply voltage



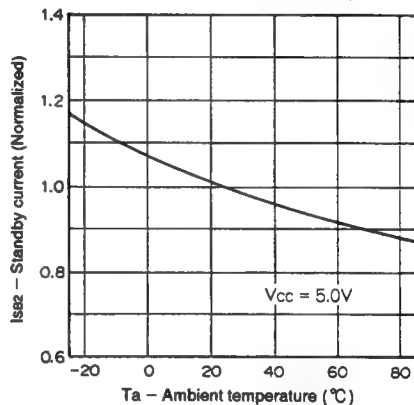
Standby current vs. Ambient temperature



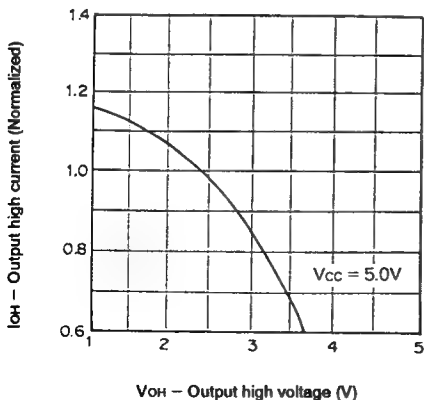
Input voltage level vs. Supply voltage



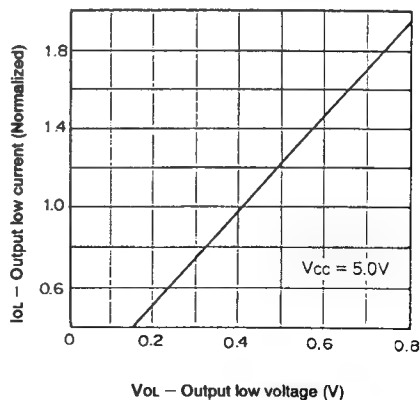
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



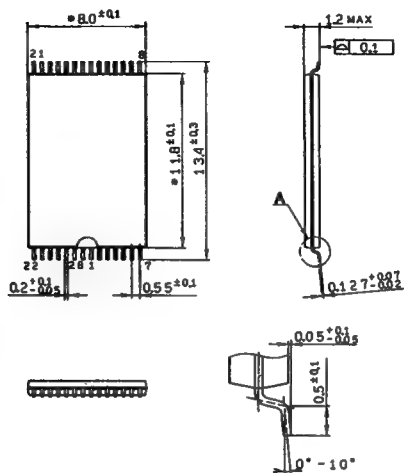
Output low current vs. Output low voltage



Package Outline Unit : mm

CXK58257ATM

28pin TSOP (Plastic)



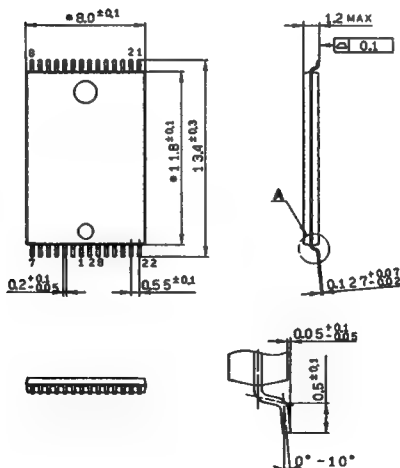
Detailed diagram of A

Note) Dimensions marked with *
do not include resin residue.

SONY NAME	TSOP-28P-L01
EIAJ NAME	TSOP028-P-0000-A
JEDEC CODE	

CXK58257AYM

28pin TSOP (Plastic)



Detailed diagram of A

Note) Dimensions marked with *
do not include resin residue.

SONY NAME	TSOP-28P-L01R
EIAJ NAME	TSOP028-P-0000-B
JEDEC CODE	

SONY**CXK58257AP/AM** -12LB**32768-word × 8-bit High Speed CMOS Static RAM****Description**

CXK58257AP/AM is a general purpose high speed CMOS static RAM organized as 32768 words by 8 bits. Operating on a single 2.7 to 5.5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

Features

- Wide supply voltage range operation: 2.7 to 5.5V
- Fast access time: (Access time)
3V \pm 10% operation; 240ns (Max.)
5V \pm 10% operation; 120ns (Max.)
- Low power consumption operation:
Standby / DC operation
3V operation; 0.75 μ W (Typ.) / 1.2mW (Typ.)
5V operation; 2.5 μ W (Typ.) / 15mW (Typ.)
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin 600mil DIP and 450mil SOP

CXK58257AP
28 pin DIP (Plastic)



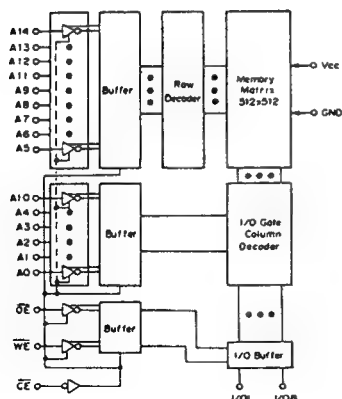
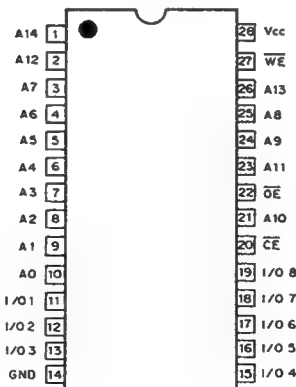
CXK58257AM
28 pin SOP (Plastic)

**Function**

32768-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block diagram**Pin Configuration**
(Top View)**Pin Description**

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
\overline{CE}	Chip enable input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
Vcc	2.7 to 5.5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK58257AP 1.0	W
		CXK58257AM 0.7	
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.**Truth Table**

CE	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	×	×	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Not selected	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	×	L	Write	Data in	I _{CC1} , I _{CC2}

× : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	V _{CC} =5V ± 10%			V _{CC} =2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V _{CC}	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	-0.3 *	—	0.4	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(GND=0V, Ta=0 to +70 °C)

Item	Symbol	Test conditions	Vcc=3V ± 10%			Vcc=5V ± 10%			Unit
			Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to Vcc	-0.5	—	0.5	-0.5	—	0.5	μA
Output leakage current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ V _{I/O} =GND to Vcc	-0.5	—	0.5	-0.5	—	0.5	μA
Operating power supply current	I _{CC1}	$\overline{CE}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	—	0.4	0.8	—	3	10	mA
		$\overline{CE} \leq 0.2V$ V _{IN} ≤ 0.2V or ≥ Vcc-0.2V							
Average operating current	I _{CC2}	Cycle=Min, Duty=100%, I _{OUT} =0mA	—	10	15	—	20	50	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$	0 to +70 °C	—	—	11	—	—	25
			0 to +40 °C	—	—	2.2	—	—	5
			+25 °C	—	0.25	1.1	—	0.5	2
	I _{SB2}	$\overline{CE}=V_{IH}$	—	0.04	0.2	—	0.4	2	mA
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.2	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	—	—	0.4	V

* Ta=25 °C

I/O Capacitance

(Ta=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

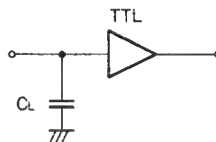
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions

(Vcc=2.7 to 5.5V, Ta=0 to +70 °C)

Item	Conditions	
	Vcc=3V	Vcc=5V
Input pulse high level	V _{IH} =2.2V	V _{IH} =2.2V
Input pulse low level	V _{IL} =0.4V	V _{IL} =0.8V
Input rise time	t _r =5ns	t _r =5ns
Input fall time	t _f =5ns	t _f =5ns
Input and output reference level	1.5V	1.5V
Output load conditions	C _L *=100pF, 1TTL	C _L *=100pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{rc}	240	—	120	—	ns
Address access time	t _{AA}	—	240	—	120	ns
Chip enable access time	t _{co}	—	240	—	120	ns
Output enable to output valid	t _{OE}	—	120	—	60	ns
Output hold from address change	t _{OH}	20	—	10	—	ns
Chip enable to output in low Z (\overline{CE})	t _{LZ}	20	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	10	—	5	—	ns
Chip disable to output in high Z (\overline{CE})	t _{HZ} *	—	60	—	30	ns
Chip disable to output in high Z (\overline{OE})	t _{OHZ} *	—	60	—	30	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

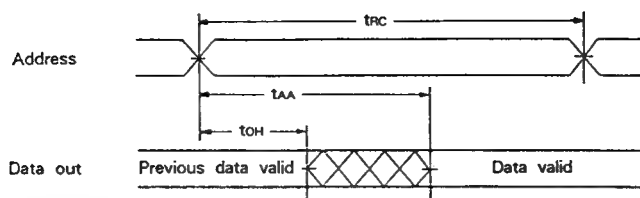
• Write cycle

Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{wc}	240	—	120	—	ns
Address valid to end of write	t _{AW}	200	—	100	—	ns
Chip enable to end of write	t _{cw}	200	—	100	—	ns
Data to write time overlap	t _{dw}	80	—	40	—	ns
Data hold from write time	t _{dH}	0	—	0	—	ns
Write pulse width	t _{WP}	140	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	ns
Write recovery time (\overline{CE})	t _{WR1}	0	—	0	—	ns
Output active from end of write	t _{OW}	20	—	10	—	ns
Write to output in high Z	t _{WHZ} *	—	50	—	25	ns

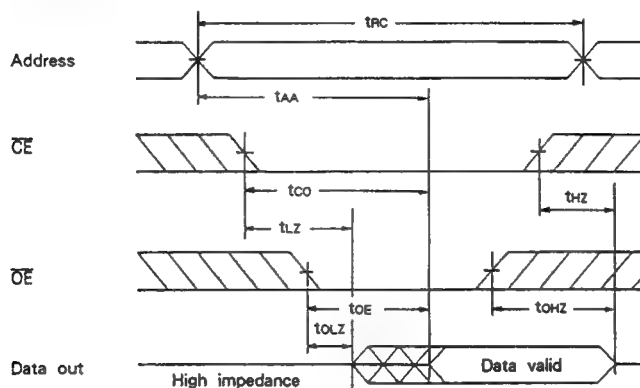
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

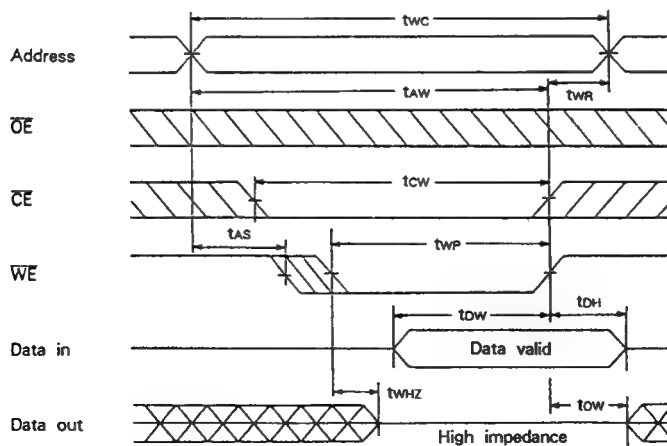
- Read cycle (1) : $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



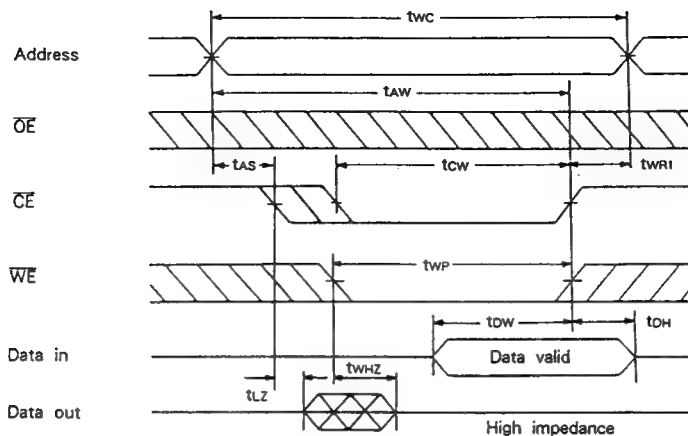
- Read cycle (2) : $\overline{WE}=V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE}}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

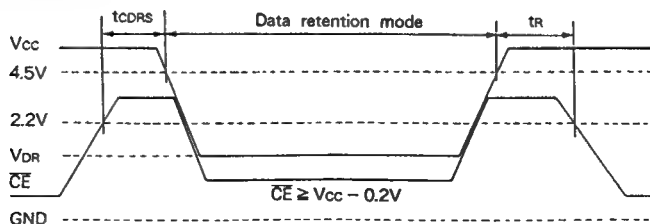
Data Retention Characteristics

($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	$\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}$	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0\text{V}$ $\overline{\text{CE}} \geq 2.8\text{V}$	0 to $+70^\circ\text{C}$	—	10	μA
			0 to $+40^\circ\text{C}$	—	2	
			$+25^\circ\text{C}$	0.25	1	
	I_{CCDR2}	$V_{CC} = 2.0$ to 5.5V , $\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}$	—	0.5	25	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		t_{RC}^*	—	—	ns

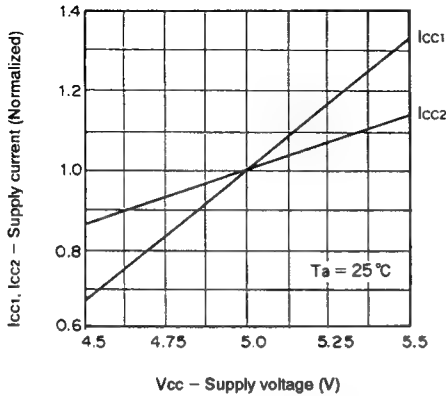
* t_{RC} : Read cycle time

Data Retention Waveform

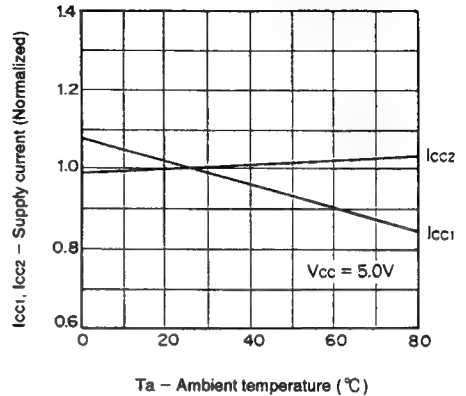


Example of Representative Characteristics

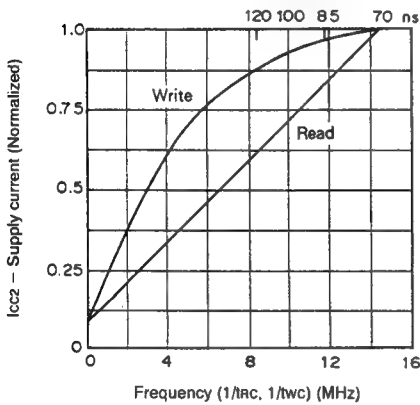
Supply current vs. Supply voltage



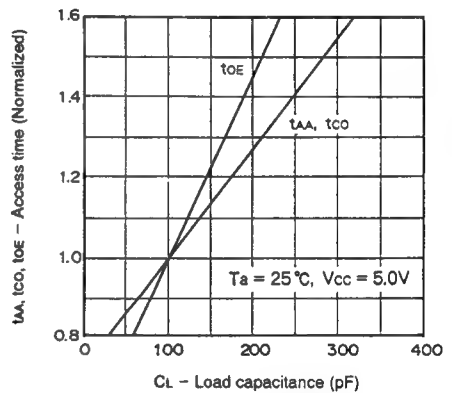
Supply current vs. Ambient temperature



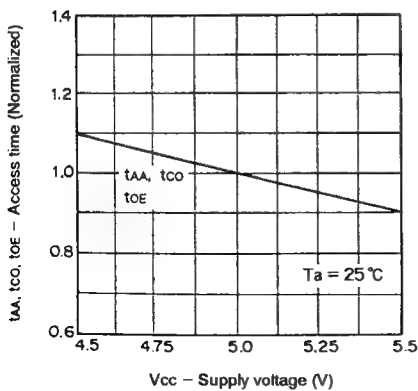
Supply current vs. Frequency



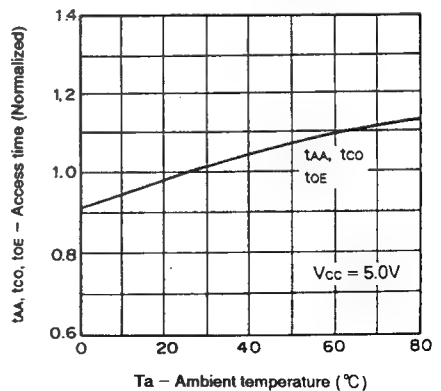
Access time vs. Load capacitance



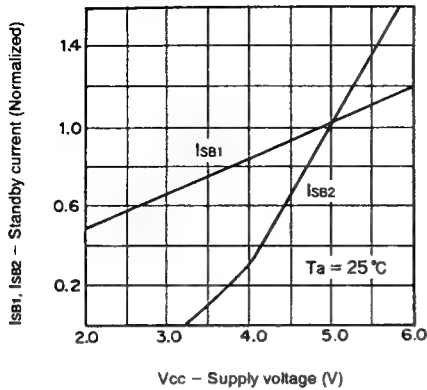
Access time vs. Supply voltage



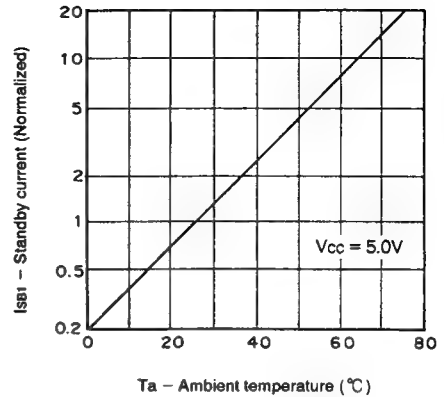
Access time vs. Ambient temperature



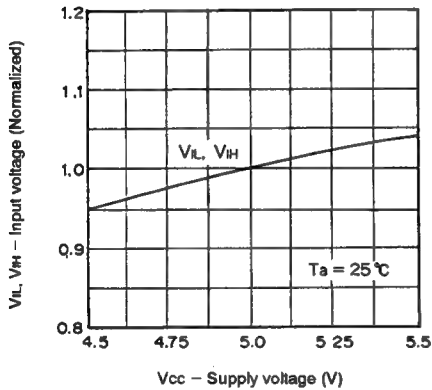
Standby current vs. Supply voltage



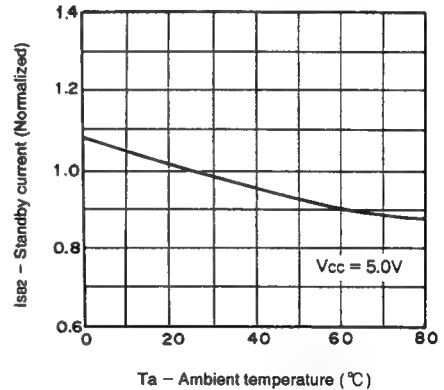
Standby current vs. Ambient temperature



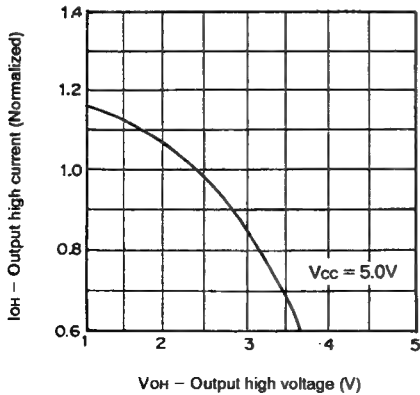
Input voltage level vs. Supply voltage



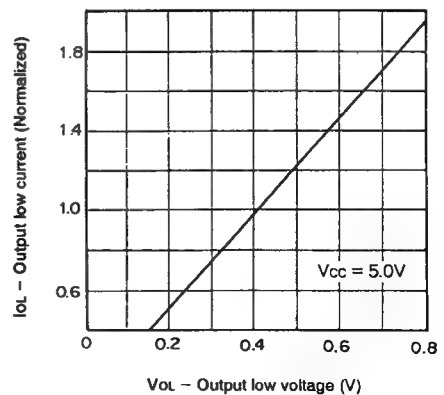
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



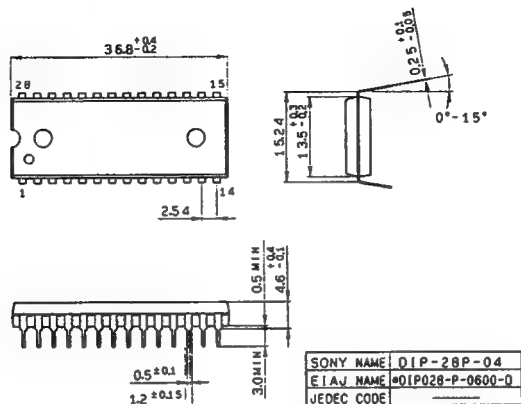
Output low current vs. Output low voltage



Package Outline Unit : mm

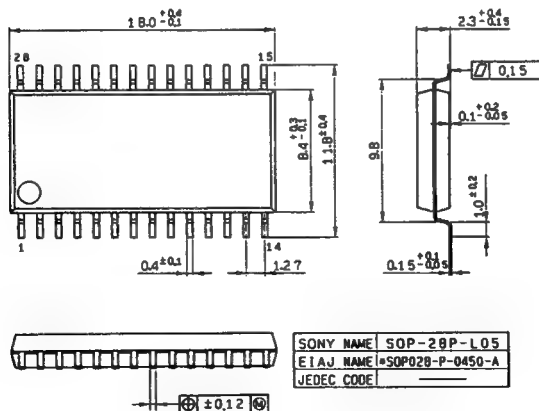
CXK58257AP

28pin DIP (Plastic) 600mil 4.2g



CXK58257AM

28pin SOP (Plastic) 450mil 0.7g



32768-word × 8-bit High Speed CMOS Static RAM

Description

CXK58257ATM/AYM is a 256K bits, 32768 words by 8 bits, CMOS static RAM. Operating on a single 2.7 to 5.5V supply. It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current.

Features

- Wide supply voltage range operation: 2.7 to 5.5V
- Thin small-outline package:

CXK58257ATM: 8mm × 13.4mm 28 pin TSOP

CXK58257AYM: 8mm × 13.4mm 28 pin TSOP

(Mirror image pinout)

- Fast access time: (Access time)
3V \pm 10% operation; 240ns (Max.)
5V \pm 10% operation; 120ns (Max.)
- Low power consumption operation:
Standby / DC operation
3V operation; 0.75 μ W (Typ.) / 1.2mW (Typ.)
5V operation; 2.5 μ W (Typ.) / 15mW (Typ.)
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)

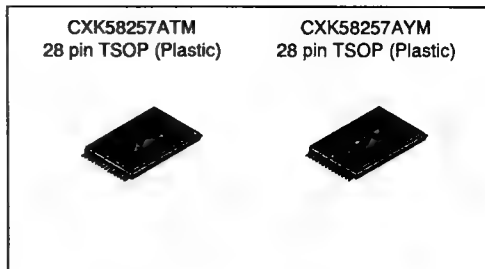
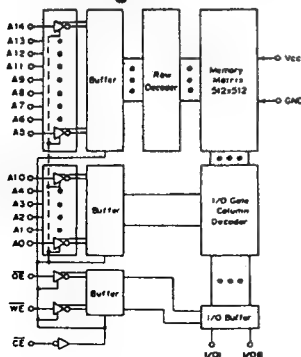
Function

32768-word \times 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram

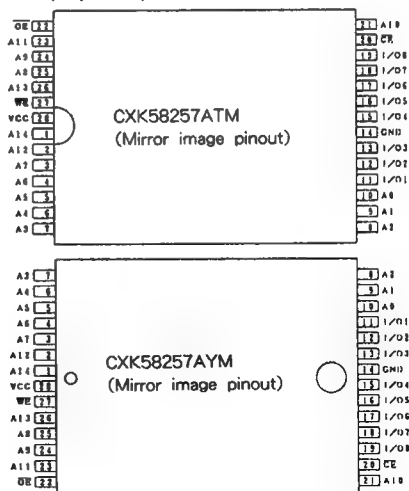


Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	2.7 to 5.5V power supply
GND	Ground

Pin Configuration

(Top View)



Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature	T _{solder}	235 ± 10	°C · sec

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.**Truth Table**

\overline{CE}	\overline{OE}	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Not selected	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	V _{CC} =5V ± 10%			V _{CC} =2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V _{CC}	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	-0.3 *	—	0.4	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions	Vcc=3V ± 10%			Vcc=5V ± 10%			Unit
			Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{II}	V _{IN} =GND to Vcc	-0.5	—	0.5	-0.5	—	0.5	μA
Output leakage current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ V _{I/O} =GND to Vcc	-0.5	—	0.5	-0.5	—	0.5	μA
Operating power supply current	I _{CC1}	$\overline{CE}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	—	0.4	0.8	—	3	10	mA
		$\overline{CE} \leq 0.2V$ V _{IN} ≤ 0.2V or ≥ Vcc-0.2V							
Average operating current	I _{CC2}	Cycle=Min, Duty=100%, I _{OUT} =0mA	—	10	15	—	20	50	mA
Standby current	I _{SB1}	$\overline{CE} \geq Vcc-0.2V$	0 to +70°C	—	—	11	—	—	μA
			0 to +40°C	—	—	2.2	—	—	
			+25°C	—	0.25	1.1	—	0.5	
	I _{SB2}	$\overline{CE}=V_{IH}$	—	0.04	0.2	—	0.4	2	mA
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.2	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	—	—	0.4	V

* Ta=25°C

I/O Capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

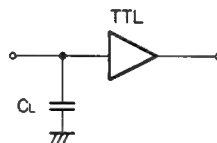
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions

(Vcc=2.7 to 5.5V, Ta=0 to +70°C)

Item	Conditions	
	Vcc=3V	Vcc=5V
Input pulse high level	V _{IH} =2.2V	V _{IH} =2.2V
Input pulse low level	V _{IL} =0.4V	V _{IL} =0.8V
Input rise time	t _r =5ns	t _r =5ns
Input fall time	t _f =5ns	t _f =5ns
Input and output reference level	1.5V	1.5V
Output load conditions	C _L * =100pF, 1TTL	C _L * =100pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	240	—	120	—	ns
Address access time	t _{AA}	—	240	—	120	ns
Chip enable access time	t _{CO}	—	240	—	120	ns
Output enable to output valid	t _{OE}	—	120	—	60	ns
Output hold from address change	t _{OH}	20	—	10	—	ns
Chip enable to output in low Z ($\overline{\text{CE}}$)	t _{LZ}	20	—	10	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ}	10	—	5	—	ns
Chip disable to output in high Z ($\overline{\text{CE}}$)	t _{HZ} *	—	60	—	30	ns
Chip disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	—	60	—	30	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

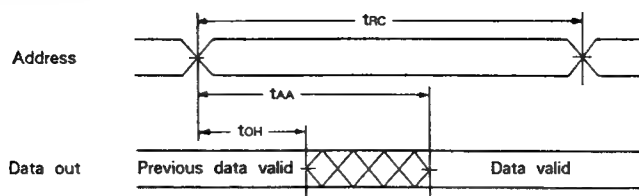
• Write cycle

Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	240	—	120	—	ns
Address valid to end of write	t _{AW}	200	—	100	—	ns
Chip enable to end of write	t _{CW}	200	—	100	—	ns
Data to write time overlap	t _{DW}	80	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	140	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	t _{WR}	0	—	0	—	ns
Write recovery time ($\overline{\text{CE}}$)	t _{WR1}	0	—	0	—	ns
Output active from end of write	t _{OW}	20	—	10	—	ns
Write to output in high Z	t _{WHZ} *	—	50	—	25	ns

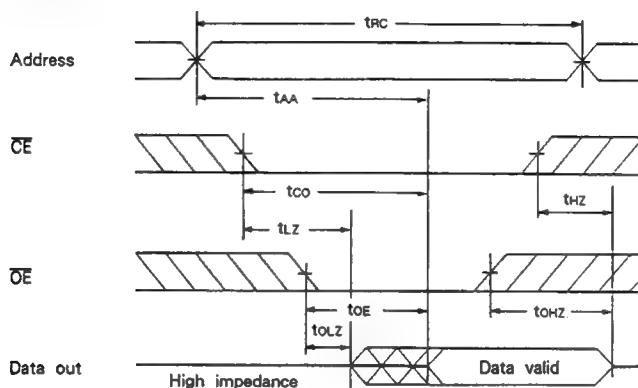
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

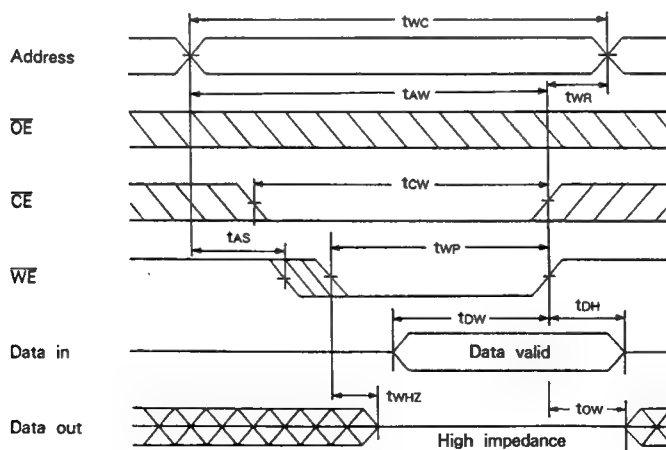
- Read cycle (1) : $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



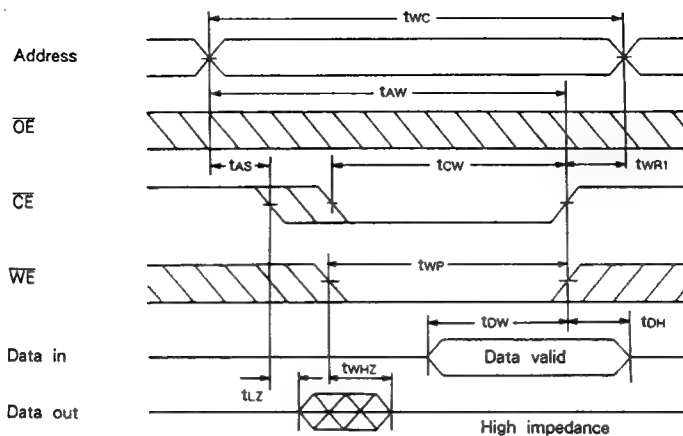
- Read cycle (2) : $\overline{WE}=V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2) : \overline{CE} control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

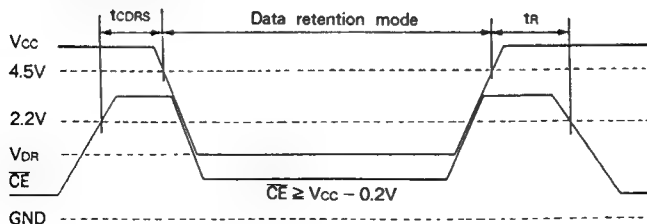
Data Retention Characteristics

($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$ $\overline{CE} \geq 2.8V$ 0 to $+70^\circ\text{C}$	—	—	10	μA
		0 to $+40^\circ\text{C}$	—	—	2	
		$+25^\circ\text{C}$	—	0.25	1	
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V$, $\overline{CE} \geq V_{CC} - 0.2V$	—	0.5	25	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		t_{RC}^*	—	—	ns

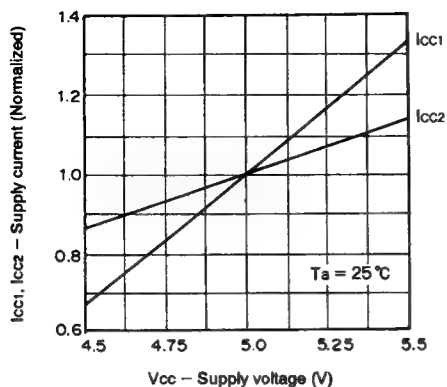
* t_{RC} : Read cycle time

Data Retention Waveform

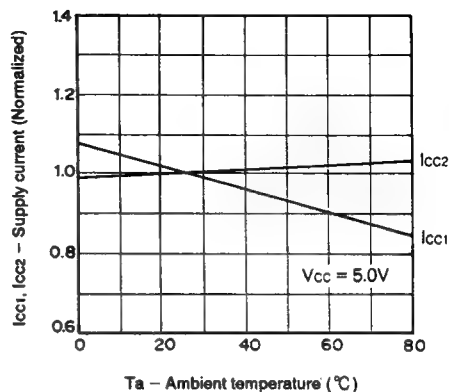


Example of Representative Characteristics

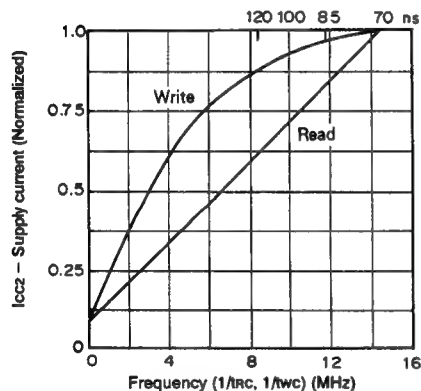
Supply current vs. Supply voltage



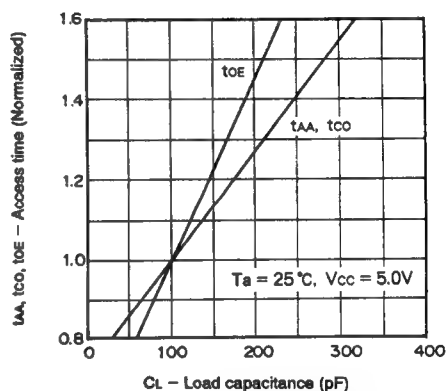
Supply current vs. Ambient temperature



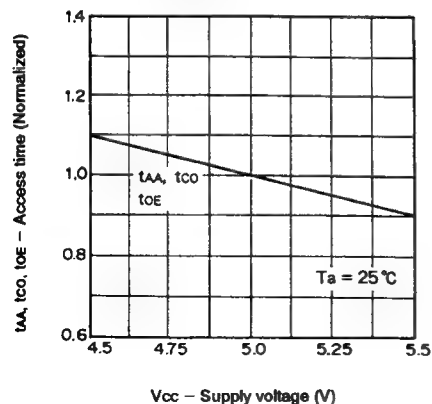
Supply current vs. Frequency



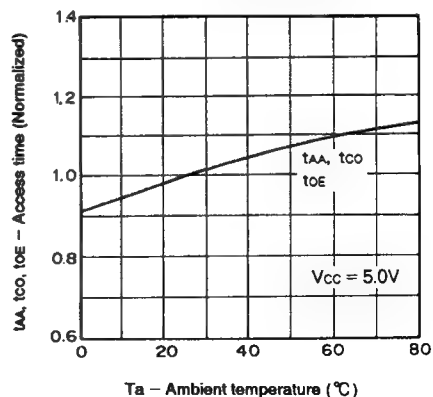
Access time vs. Load capacitance



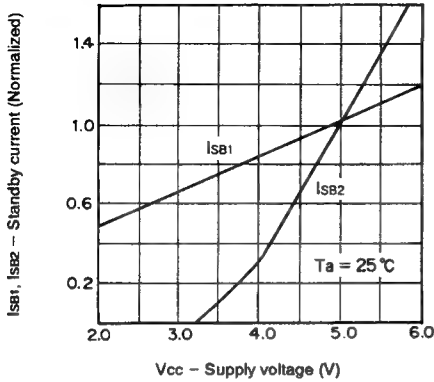
Access time vs. Supply voltage



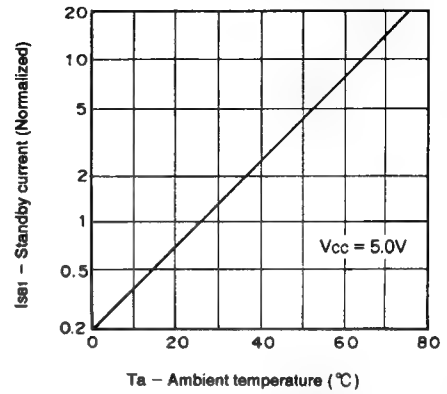
Access time vs. Ambient temperature



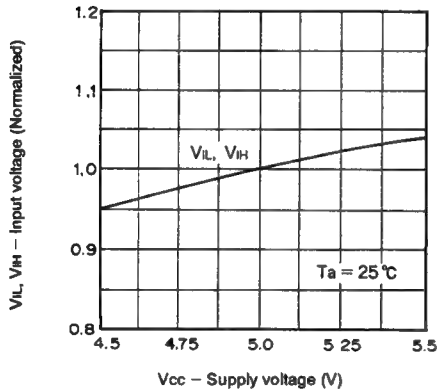
Standby current vs. Supply voltage



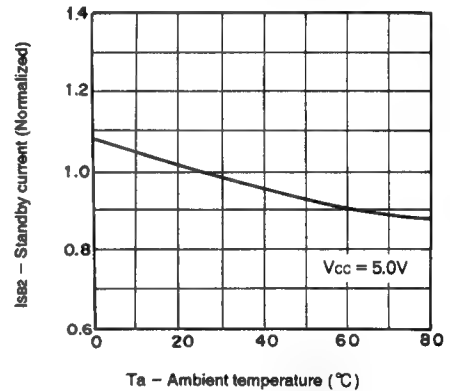
Standby current vs. Ambient temperature



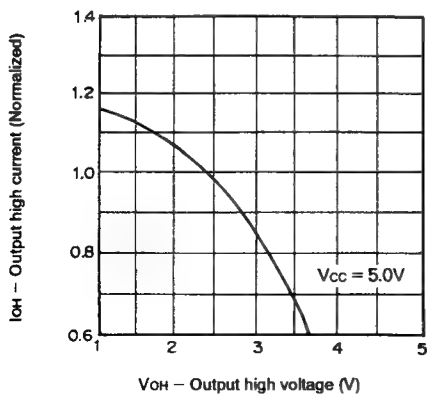
Input voltage level vs. Supply voltage



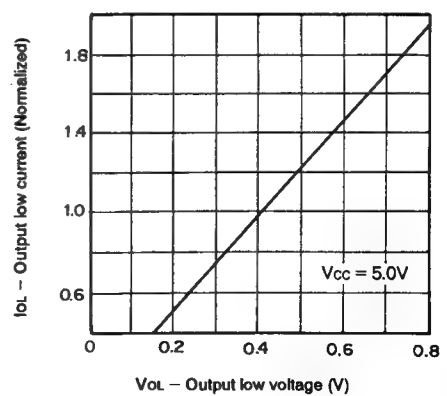
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



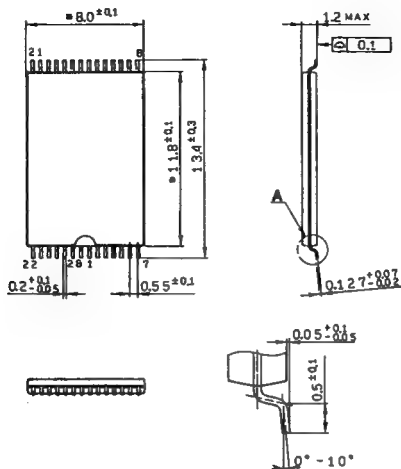
Output low current vs. Output low voltage



Package Outline Unit : mm

CXK58257ATM

28pin TSOP (Plastic)



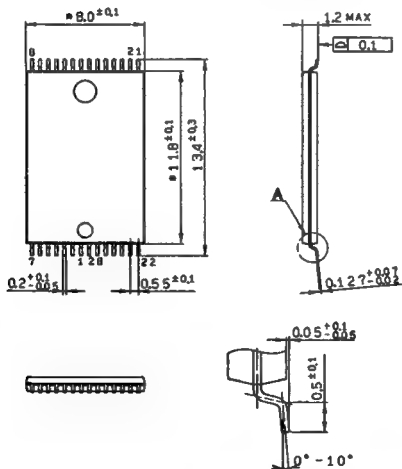
Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.

SONY NAME	TSOP-28P-L01
EIAJ NAME	TSOP028-P-0000-A
JEDEC CODE	

CXK58257AYM

28pin TSOP (Plastic)



Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.

SONY NAME	TSOP-28P-L01R
EIAJ NAME	TSOP028-P-0000-B
JEDEC CODE	

SONY**CXK58258AP/AJ** -15*/20/25/35****32,768-word × 8-bit High Speed CMOS Static RAM** *under development
Only SOJ availableDescription**

The CXK58258AP/AJ is a high speed CMOS static RAM which consists of 32,768-word × 8-bit. It operates at 15/20/25/35ns access time from 5V single power supply.

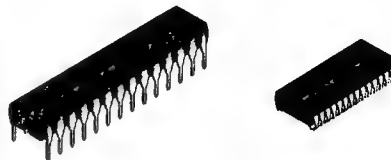
Features

- High speed, low power consumption :

	Access time (Max.)	Power consumption (Typ., Cycle = Min.)
CXK58258AP/AJ-15	15ns	500mW
CXK58258AP/AJ-20	20ns	400mW
CXK58258AP/AJ-25	25ns	350mW
CXK58258AJ-35	35ns	300mW

- Single +5V power supply :
 - 15 5V ± 5%
 - 20/25/35 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible all inputs and outputs.
- Common data input and output :
three state output
- Available in 28 pin 300mil DIP, 300mil SOJ package.

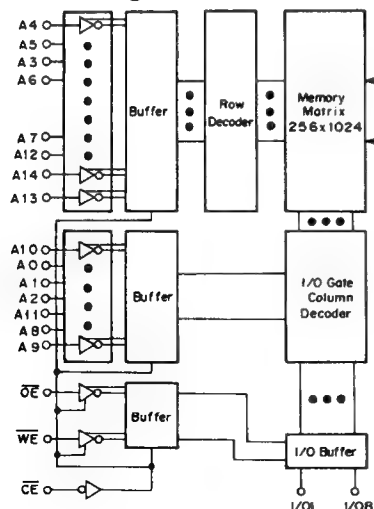
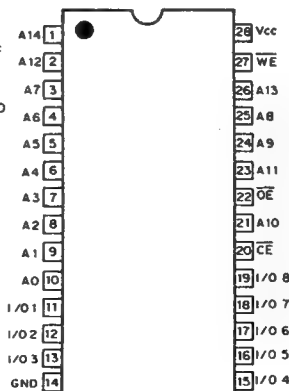
CXK58258AP 28 pin DIP (Plastic) CXK58258AJ 28 pin SOJ (Plastic)

**Function**

32,768-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration**
(Top view)**Pin Description**

Symbol	Description
A0 to A14	Address input
I/O 1 to I/O 8	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5* to +7.0	V
Input voltage	V _{IN}	-0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	-0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} = -3.5V Min. for pulse width less than 20ns.**Truth Table**

CE	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	X	L	Write	Data in	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	-15	4.75	5.0	V
		-20/25/35	4.5	5.0	
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

* V_{IL} = -3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%*, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.**	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	1	μA
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , CE = V _{IH} or OE = V _{IH} or WE = V _{IL}	-1	—	1	μA
Operating power supply current	I _{CC1}	CE = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	—	—	mA
Average operating current	I _{CC2}	Cycle = Min, Duty = 100%, I _{OUT} = 0mA, CE = V _{IL} , V _{IN} = V _{IH} or V _{IL}	-15	100	140	mA
			-20	80	120	
			-25	70	120	
			-35	60	100	
Standby current	I _{SB1}	CE ≥ V _{CC} - 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	1	mA
	I _{SB2}	Cycle = Min, Duty = 100%, CE = V _{IH} , V _{IN} = V _{IL} or V _{IH}	—	20	30	mA
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V ± 5% for CXK58258AP/AJ-15** V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

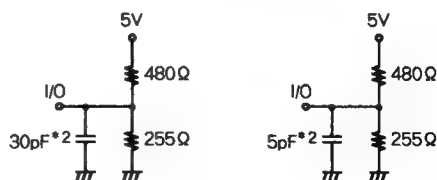
AC characteristics

• AC test conditions

(V_{CC} = 5V ± 10%*, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 3ns
Input fall time	t _f = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load(1) Output Load(2)*3

*1 V_{CC} = 5V ± 5% for CXK58258AP/AJ-15

*2 including scope and jig capacitance

*3 for t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	- 15		- 20		- 25		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	15	—	20	—	25	—	35	—	ns
Address access time	t _{AA}	—	15	—	20	—	25	—	35	ns
Chip enable access time	t _{CO}	—	15	—	20	—	25	—	35	ns
Output enable to output valid	t _{OE}	—	8	—	10	—	12	—	12	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	5	—	ns
Chip enable to output in low Z (\overline{CE})	t _{LZ} *	3	—	3	—	3	—	3	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ} *	2	—	2	—	2	—	2	—	ns
Chip disable to output in high Z (\overline{CE})	t _{HZ} *	—	8	—	9	—	10	—	10	ns
Output disable to output in high Z (\overline{OE})	t _{OHZ} *	—	7	—	8	—	9	—	9	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	0	—	ns
Chip disable to power down	t _{PD}	—	15	—	20	—	25	—	35	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

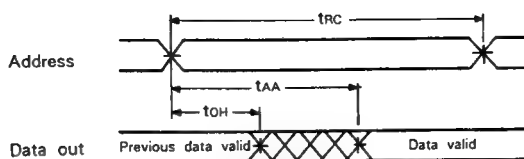
• Write cycle

Item	Symbol	- 15		- 20		- 25		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	15	—	20	—	25	—	35	—	ns
Address valid to end of write	t _{AW}	11	—	13	—	15	—	15	—	ns
Chip enable to end of write	t _{CW}	12	—	14	—	16	—	16	—	ns
Data to write time overlap	t _{DW}	9	—	11	—	12	—	12	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	10	—	13	—	15	—	15	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (\overline{CE})	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	3	—	3	—	3	—	3	—	ns
Write to output in high Z	t _{WHZ} *	—	8	—	9	—	10	0	10	ns

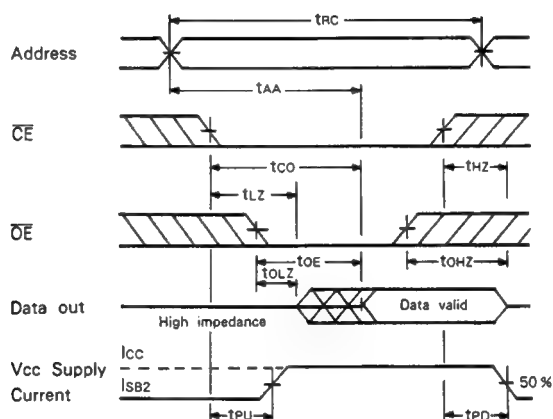
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

Timing Waveform

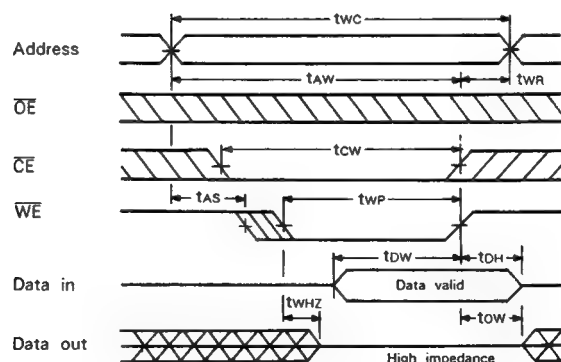
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



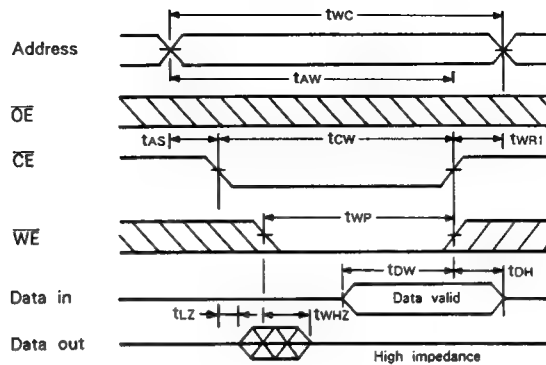
- Read cycle (2) : $\overline{WE} = V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE}}$ control



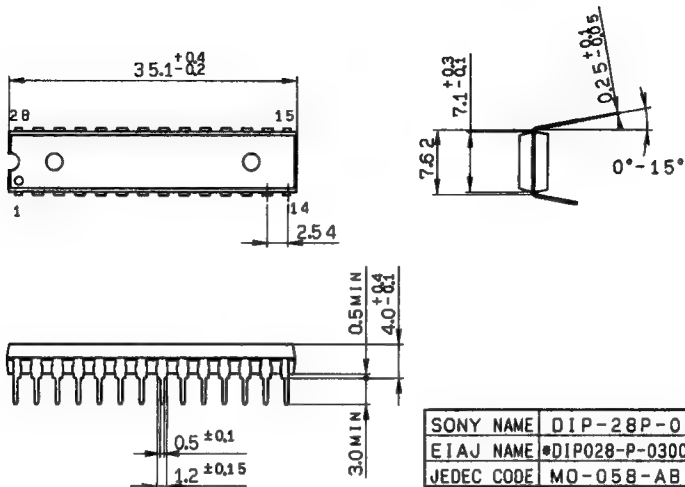
Note)

1. Write occurs during the low overlap of $\overline{\text{CE}}$ and $\overline{\text{WE}}$.
2. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

CXK58258AP

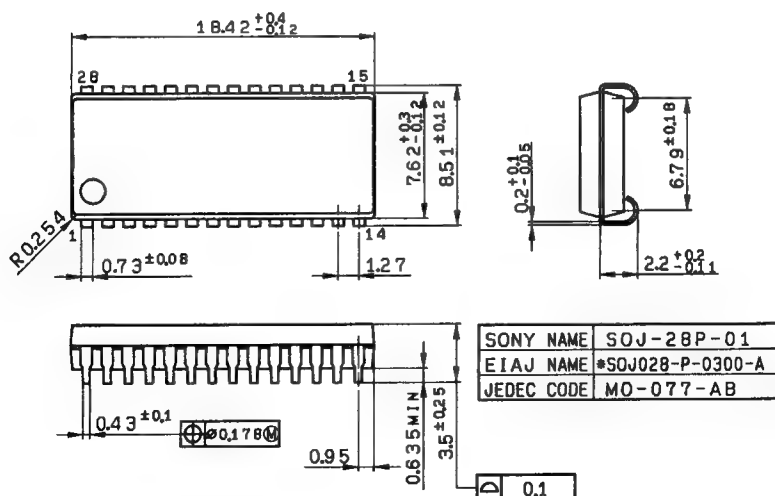
28pin DIP (Plastic) 300mil 2.0g



* (Similar)

CXK58258AJ

28pin SOJ (Plastic) 300mil 0.8g



SONY CXK58258BP/BJ/BM* -20L*/25L/35L -20LL*/25LL/35LL

32,768-word × 8-bit High Speed CMOS Static RAM * under development

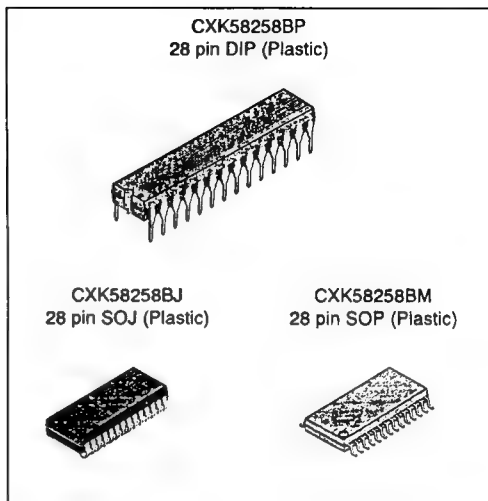
Description

The CXK58258BP/BJ/BM is a high speed CMOS static RAM which consists of 32,768-word × 8-bit. It operates at 20/25/35ns access time from 5V single power supply.

This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time (Access time)
CXK58258BP/BJ/BM-20L, 20LL 20ns (Max.)
CXK58258BP/BJ/BM-25L, 25LL 25ns (Max.)
CXK58258BP/BJ/BM-35L, 35LL 35ns (Max.)
- Low power operation Standby Operation
(Max.) (Typ., Min. Cycle)
CXK58258BP/BJ/BM-20LL 5 μ W 400mW
CXK58258BP/BJ/BM-25LL 5 μ W 350mW
CXK58258BP/BJ/BM-35LL 5 μ W 300mW
CXK58258BP/BJ/BM-20L 10 μ W 400mW
CXK58258BP/BJ/BM-25L 10 μ W 350mW
CXK58258BP/BJ/BM-35L 10 μ W 300mW
- Single +5V power supply: 5V \pm 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible all inputs and outputs.
- Common data input and output:three state output
- Available in 28 pin 300mil DIP, 300mil SOJ, 450mil SOP package.



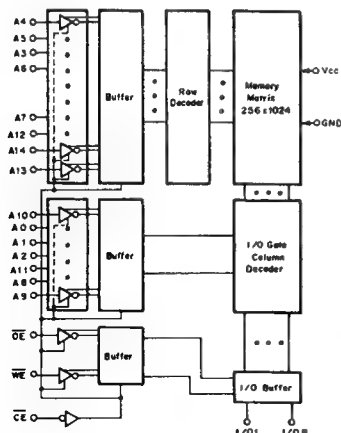
Function

32,768-word × 8-bit static RAM

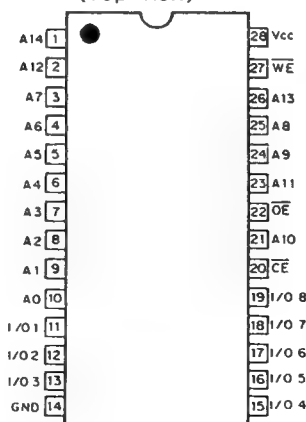
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
\overline{CE}	Chip enable input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 * to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{IO}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK58258BP/BJ	1.0
		CXK58258BM	0.7
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{IO} = -3.5V Min. for pulse width less than 20ns.**Truth Table**

\overline{CE}	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O8	V _{CC} Current
H	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	x	L	Write	Data in	I _{CC1} , I _{CC2}

x : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL} = -3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70 °C)

Item	Symbol	Test conditions		-20L/25L/35L			-20LL/25LL/35LL			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	V _{IO} =GND to V _{CC} , CE=V _{IH} or OE=V _{IH}		-1	—	1	-1	—	1	μA
Operating power supply current	I _{CC1}	CE=V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA		—	—	—	—	—	—	mA
Average operating current	I _{CC2}	Cycle=Min, Duty=100%, I _{OUT} =0mA, CE=V _{IL} , V _{IN} =V _{IH} or V _{IL}	-20L/20LL	—	80	120	—	80	120	mA
			-25L/25LL	—	70	120	—	70	120	
			-35L/35LL	—	60	100	—	60	100	
Standby current	I _{SB1}	CE ≥ V _{CC} -0.2V		—	0.002	0.1	—	0.001	0.05	mA
	I _{SB2}	Cycle=Min, Duty=100%, CE=V _{IH}		—	1.5	5	—	1.5	5	mA
Output high voltage	V _{OH}	I _{OH} = -4.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =8.0mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25 °C

I/O capacitance

(Ta=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{IO} =0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

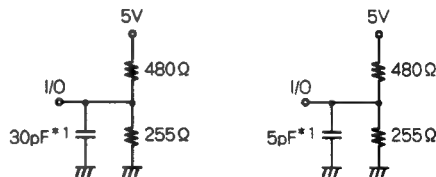
AC characteristics

• AC test conditions

(Vcc=5V ± 10%, Ta=0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} =3.0V
Input pulse low level	V _{IL} =0V
Input rise time	tr=3ns
Input fall time	tf=3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1) Output Load (2) *2



* 1 including scope and jig capacitance

* 2 for tLZ, tHZ, tOHZ, tOLZ, tOW, tWHZ

Fig. 1

• Read cycle

Item	Symbol	-20L/20LL		-25L/25LL		-35L/35LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	20	—	25	—	35	—	ns
Address access time	t _{AA}	—	20	—	25	—	35	ns
Chip enable access time	t _{CC}	—	20	—	25	—	35	ns
Output enable to output valid	t _{OE}	—	10	—	12	—	15	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{\text{CE}}$)	t _{LZ} *	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ} *	2	—	2	—	2	—	ns
Chip disable to output in high Z ($\overline{\text{CE}}$)	t _{HZ} *	—	9	—	10	—	15	ns
Output disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	—	8	—	9	—	12	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	20	—	25	—	35	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

This parameter is sampled and is not 100% tested.

• Write cycle

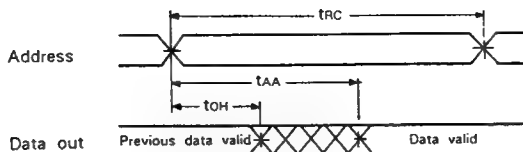
Item	Symbol	-20L/20LL		-25L/25LL		-35L/35LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	20	—	25	—	35	—	ns
Address valid to end of write	t _{AW}	13	—	15	—	20	—	ns
Chip enable to end of write	t _{CW}	14	—	16	—	20	—	ns
Data to write time overlap	t _{DW}	11	—	12	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	13	—	15	—	20	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{CE}}$)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	3	—	3	—	3	—	ns
Write to output in high Z	t _{WHZ} *	—	9	—	10	—	12	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

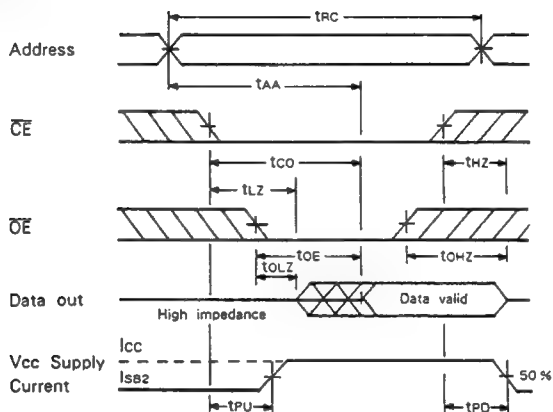
This parameter is sampled and is not 100% tested.

Timing Waveform

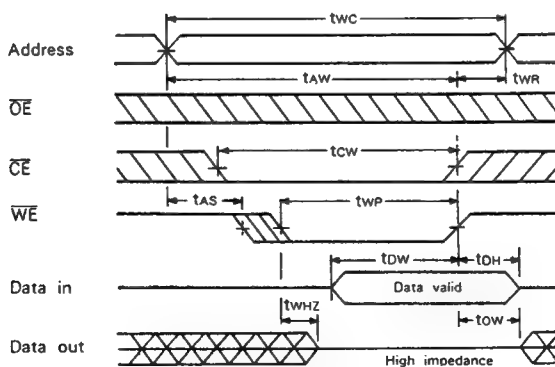
- Read cycle (1): $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



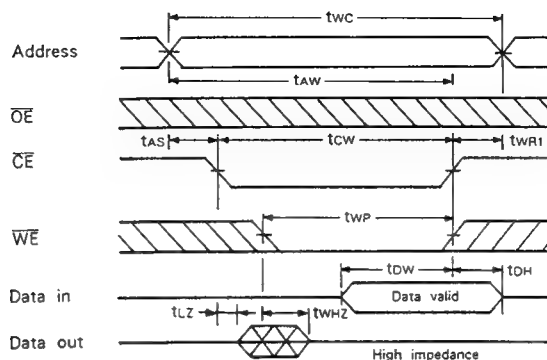
- Read cycle (2): $\overline{WE}=V_{IH}$



- Write cycle (1): \overline{WE} control



• Write cycle (2): \overline{CE} control



Note)

1. Write occurs during the low overlap of \overline{CE} and \overline{WE} .
2. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

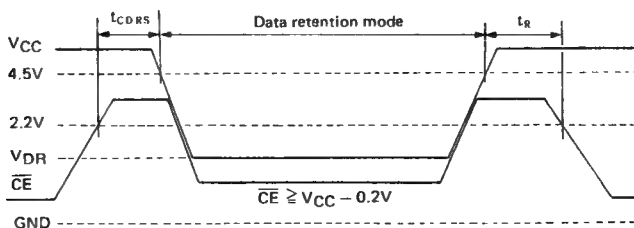
Data Retention Characteristics

($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test conditions		-20L/25L/35L			-20LL/25LL/35LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	$\overline{CE} \geq V_{CC}-0.2V$		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V CE ≥ 2.8V	Ta=0 to 70 °C	—	—	50	—	—	10	μA
			Ta=0 to 40 °C	—	—	10	—	—	4	
			25 °C	—	1	3	—	0.5	1	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V CE ≥ V _{CC} – 0.2V	—	0.002	0.1	—	0.001	0.05	mA	
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t _R			t _{RC} *	—	—	t _{RC} *	—	—	ns

* t_{RC} : Read cycle time

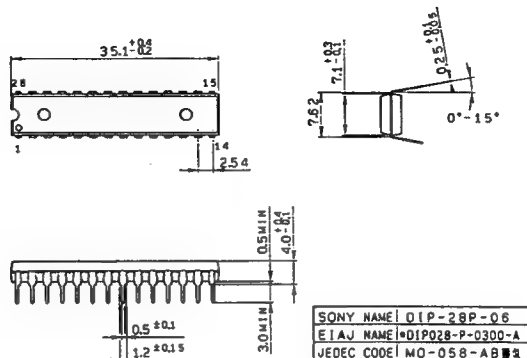
Data retention time



Package Outline Unit : mm

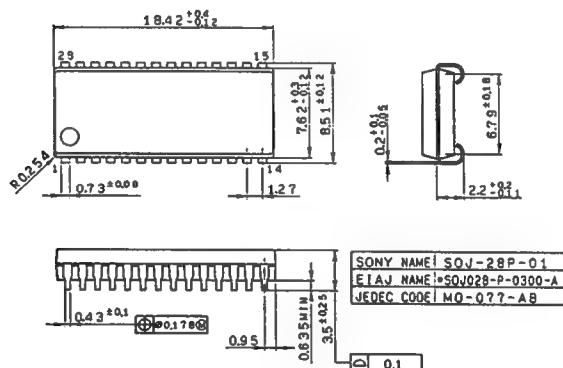
CXK58258BP

28pin DIP (Plastic) 300mil 2.0g



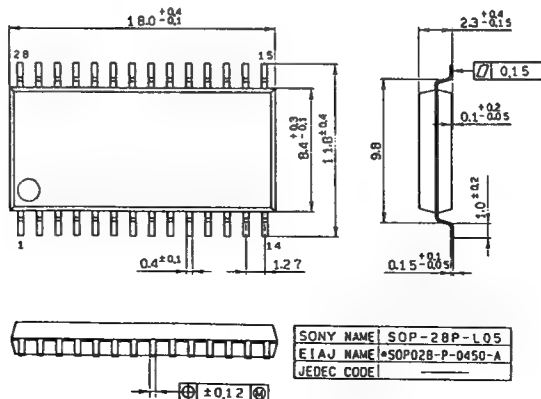
CXK58258BJ

28pin SOJ (Plastic) 300mil 0.8g



CXK58258BM

28pin SOP (Plastic) 450mil 0.7g



SONY**CXK58267AM** -70L/85L/10L/12L
-70LL/85LL/10LL/12LL**32768-word × 8-bit High Speed CMOS Static RAM****Description**

CXK58267AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. The CXK58267AM's two chip enable inputs are useful for battery back up operation for nonvolatility.

Features

- Fast access time: (Access time)
CXK58267AM-70L,70LL 70ns (Max.)
CXK58267AM-85L,85LL 85ns (Max.)
CXK58267AM-10L,10LL 100ns (Max.)
CXK58267AM-12L,12LL 120ns (Max.)
- Low power operation:
CXK58267AM-70LL,85LL,10LL,12LL;
Standby : 1 μ W (Typ.)
Operation : 15mW (Typ.)
CXK58267AM-70L,85L,10L,12L;
Standby : 2.5 μ W (Typ.)
Operation : 15mW (Typ.)
- Single +5V supply: +5V \pm 10%
- Fully static memory...No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin SOP

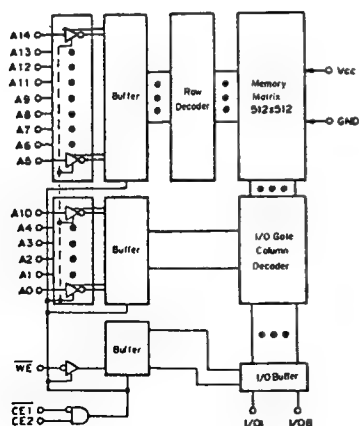
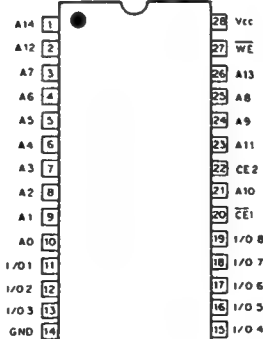
28 pin SOP (Plastic)

**Function**

32768-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration
(Top View)****Pin Description**

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{IO}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{IO}=-3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions		-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _I	V _{IN} =GND to V _{CC}		-0.5	—	0.5	-0.5	—	0.5	μA
Output leakage current	I _{LO}	$\overline{CE1}=V_{IH}$ or CE2=V _{IL} or $\overline{WE}=V_{IL}$, V _{I/O} =GND to V _{CC}		-0.5	—	0.5	-0.5	—	0.5	μA
Operating power supply current	I _{CC1}	$\overline{CE1}=V_{IL}$, CE2=V _{IH} , I _{OUT} =0mA		—	3	10	—	3	10	mA
		$\overline{CE1}=0.2V$, CE2=V _{CC} -0.2V V _{IN} =0.2V or V _{CC} -0.2V		—	1	5	—	1	5	
Average operating current	I _{CC2}	Min. cycle Duty=100%, I _{OUT} =0mA	70L/70LL	—	30	50	—	30	50	mA
			85L/85LL	—	25	50	—	25	50	
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I _{SB1}	CE2 ≤ 0.2V or $\left(\begin{array}{l} \overline{CE1} \geq V_{CC}-0.2V \\ CE2 \geq V_{CC}-0.2V \end{array} \right)$	0 to 70 °C	—	—	25	—	—	5	μA
			0 to 40 °C	—	—	5	—	—	1	
			25 °C	—	0.5	2	—	0.2	0.5	
		I _{SB2}	CE2=V _{IL} , or $\overline{CE1}=V_{IH}$		—	0.6	3	—	0.6	3
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

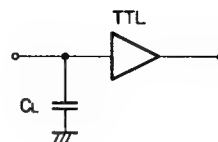
(T_a=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics**● AC test conditions**(V_{CC}=5V ± 10%, T_a=0 to +70°C)

Item		Conditions
Input pulse high level		V _{IH} =2.2V
Input pulse low level		V _{IL} =0.8V
Input rise time		t _r =5ns
Input fall time		t _f =5ns
Input and output reference level		1.5V
Output load conditions	85L/85LL/10L/10LL/12L/12LL	C _L * =100pF, 1TTL
	70L/70LL	C _L * =30pF, 1TTL

* C_L Includes scope and jig capacitances.

• Read cycle

Item	Symbol	- 70L/70LL		- 85L/85LL		- 10L/10LL		- 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time (CE1, CE2)	t _{CO1} , t _{CO2}	—	70	—	85	—	100	—	120	ns
Output hold from address change	t _{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	10	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	0	30	0	30	0	30	0	30	ns

* t_{HZ1} and t_{HZ2} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

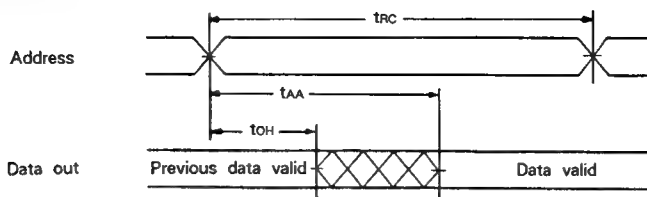
• Write cycle

Item	Symbol	- 70L/70LL		- 85L/85LL		- 10L/10LL		- 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

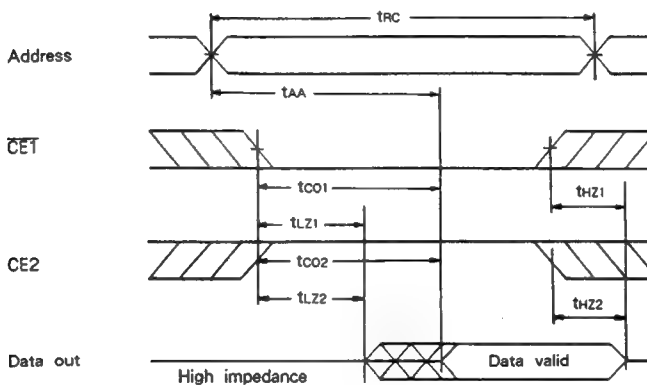
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

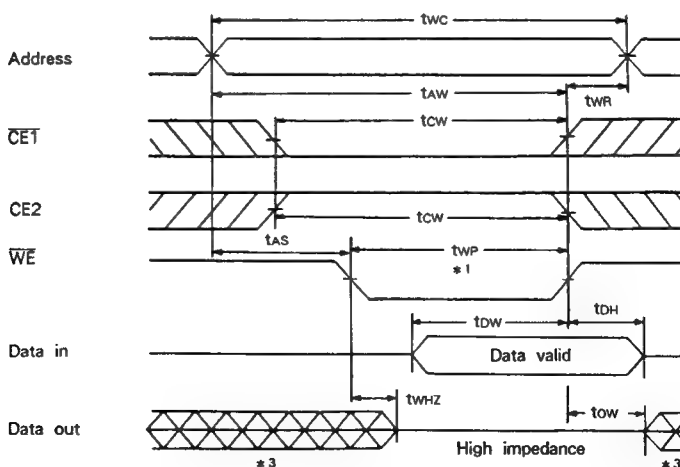
- Read cycle (1) : $\overline{CE1}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



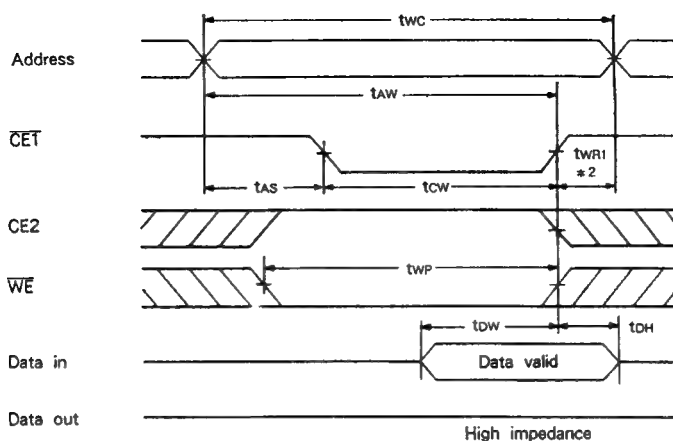
- Read cycle (2) : $\overline{WE}=V_{IH}$



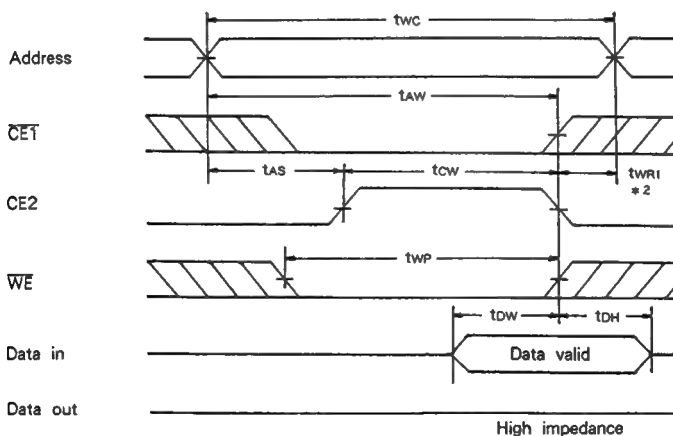
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



- * 1. A write occurs during the period of $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ being low and CE2 being high.
- * 2. t_{WR1} is measured from the earlier of $\overline{\text{CE1}}$ or $\overline{\text{WE}}$ going high and CE2 going low to the end of write cycle.
- * 3. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

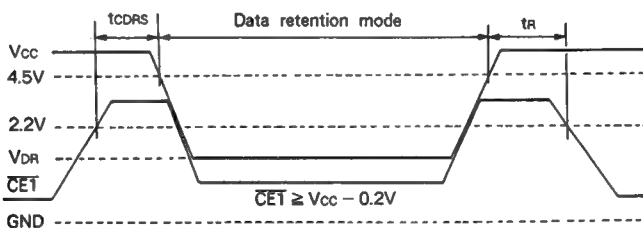
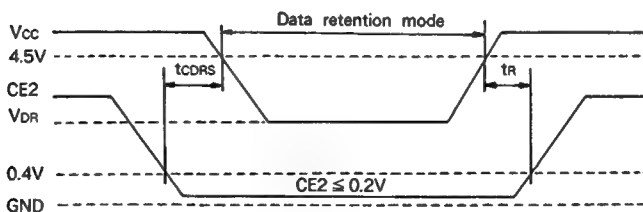
Data Retention Characteristics

(Ta=0 to 70 °C)

Item	Symbol	Test conditions		- 70L/85L/10L/12L			- 70LL/85LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V *1	0 to 70 °C	—	—	10	—	—	3	μA
			0 to 40 °C	—	—	2	—	—	0.6	
			25 °C	—	0.25	1	—	0.1	0.3	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V *1		—	0.5	25	—	0.2	5	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t _R			t _{RC} *2	—	—	t _{RC} *2	—	—	ns

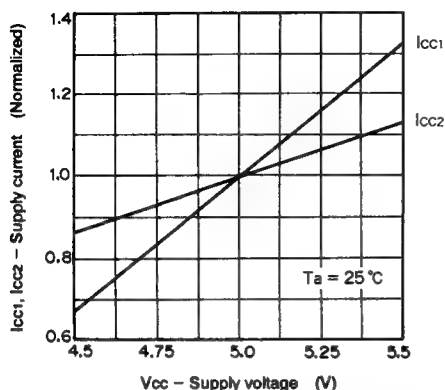
*1. $\overline{CE1} \geq V_{CC}-0.2V$, $CE2 \geq V_{CC}-0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)*2. t_{RC}: Read cycle time

Data retention waveform

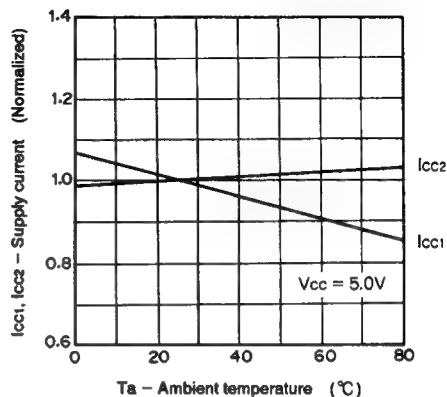
• Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)• Low supply voltage data retention waveform (2) ($CE2$ control)

Example of Representative Characteristics

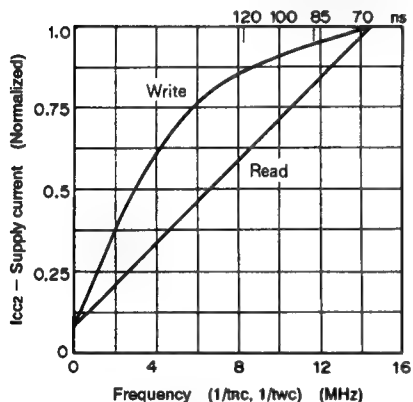
Supply current vs. Supply voltage



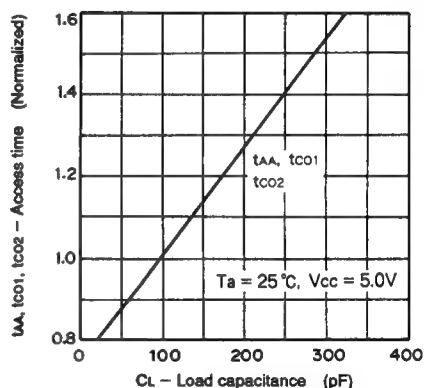
Supply current vs. Ambient temperature



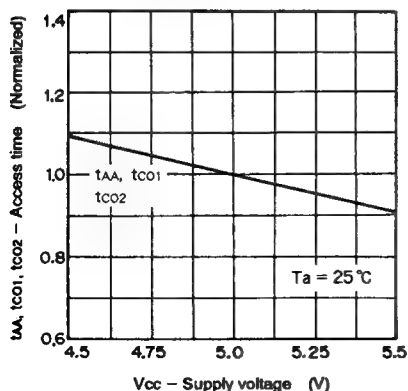
Supply current vs. Frequency



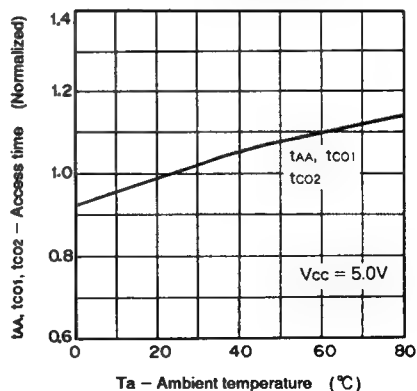
Access time vs. Load capacitance



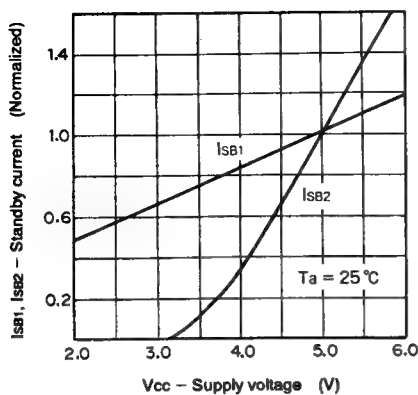
Access time vs. Supply voltage



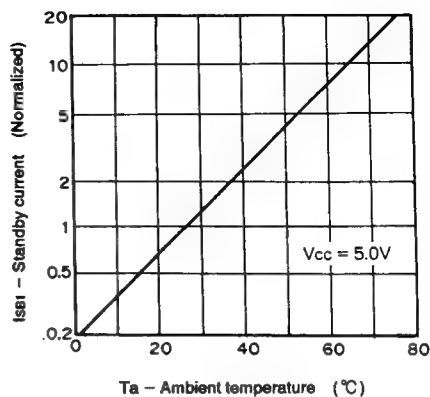
Access time vs. Ambient temperature



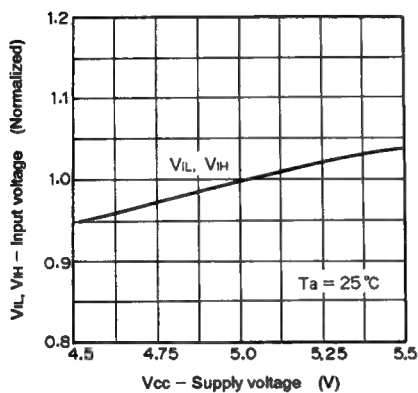
Standby current vs. Supply voltage



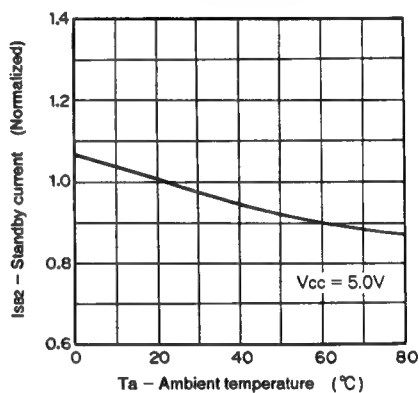
Standby current vs. Ambient temperature



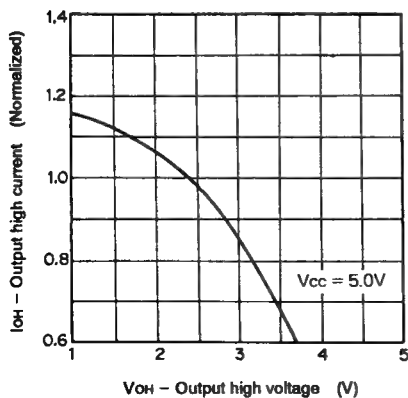
Input voltage level vs. Supply voltage



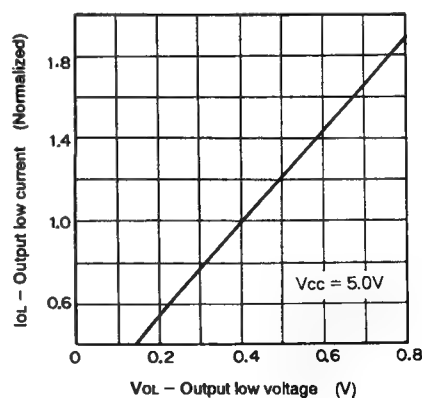
Standby current vs. Ambient temperature



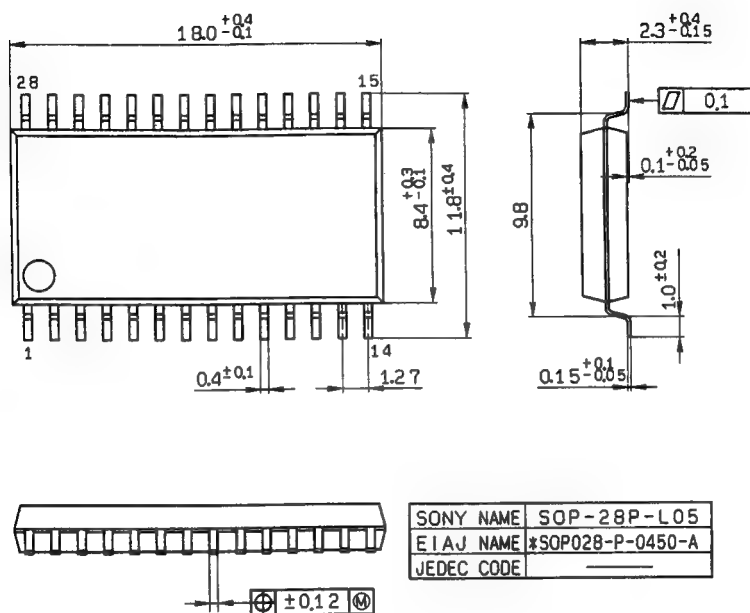
Output high current vs. Output high voltage



Output low current vs. Output low voltage



Package Outline Unit : mm



SONY CXK58267ATM/AYM -70L/85L/10L/12L

32768-word × 8-bit High Speed CMOS Static RAM

Description

CXK58267ATM/AYM is a 256K bits, 32768 words by 8 bits, CMOS static RAM. It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current. It has two chip enable control inputs, $\overline{CE1}$ & $\overline{CE2}$, which allow to achieve multiple memory use with battery back-up applications.

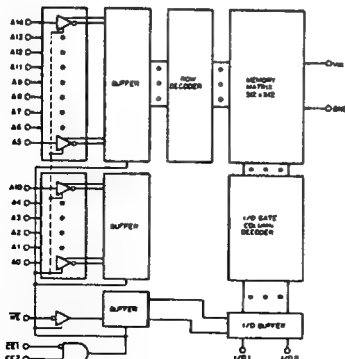
Features

- Two Chips Enable Control Inputs
Provide Stand-by/Data Retention Mode
 $\overline{CE1}$: Low Active
 $\overline{CE2}$: High Active
- Thin Small-outline Packages :
CXK58267ATM: 8mm × 13.4mm 28 pin TSOP
CXK58267AYM: 8mm × 13.4mm 28 pin TSOP (Mirror image pinout)
- Low stand-by current :
25 μ A (Max.) @ $V_{CC} = 5.5V$, $T_a = 0$ to $70^\circ C$
- Low voltage data retention: 2.0V (Min.)
- Fast access time : (Access time)
CXK58267ATM/AYM-70L 70ns (Max.)
CXK58267ATM/AYM-85L 85ns (Max.)
CXK58267ATM/AYM-10L 100ns (Max.)
CXK58267ATM/AYM-12L 120ns (Max.)
- Single +5V Supply : +5V \pm 10%

Function

32768-word × 8-bit static RAM

Block Diagram



CXK58267ATM 28 pin TSOP (Plastic) CXK58267AYM 28 pin TSOP (Plastic)



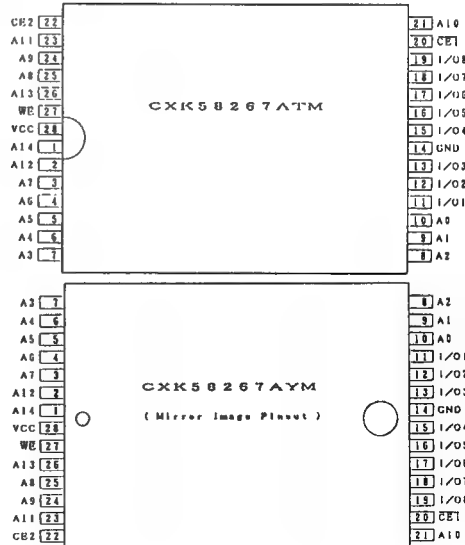
Structure

Silicon gate CMOS IC

Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, $\overline{CE2}$	Chip enable 1, 2 input
WE	Write enable input
Vcc	+5V power supply
GND	Ground

Pin Configuration (Top View)



Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK58267AP/ASP	1.0
		CXK58267AM	0.7
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
x	L	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	L	Write	Data in	I _{CC1} , I _{CC2}

x : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics ($V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0$ to $+70^\circ C$)

Item	Symbol	Test conditions		- 70L/85L/10L/12L			Unit
				Min.	Typ.*	Max.	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}		- 0.5	—	0.5	μA
Output leakage current	I _{LO}	$\overline{CE1} = V_{IH}$ or CE2 = V _{IL} or $\overline{WE} = V_{IL}$, V _{I/O} = GND to V _{CC}		- 0.5	—	0.5	μA
Operating power supply current	I _{CC1}	$\overline{CE1} = V_{IL}$, CE2 = V _{IH} , I _{OUT} = 0mA		—	3	10	mA
		$\overline{CE1} = 0.2V$, CE2 = V _{CC} - 0.2V V _{IN} = 0.2V or V _{CC} - 0.2V		—	1	5	
Average operating current	I _{CC2}	Min. cycle Duty = 100 %, I _{OUT} = 0mA	70L	—	30	50	mA
			85L	—	25	50	
			10L	—	23	50	
			12L	—	20	50	
Standby current	I _{SB1}	CE2 ≤ 0.2V or $\left(\overline{CE1} \geq V_{CC} - 0.2V \right.$ $\left. CE2 \geq V_{CC} - 0.2V \right)$	0 to 70°C	—	—	25	μA
			0 to 70°C	—	—	5	
			25°C	—	0.5	2	
	I _{SB2}	CE2 = V _{IL} , or $\overline{CE1} = V_{IH}$		—	0.6	3	mA
Output high voltage	V _{OH}	I _{OH} = - 1.0mA		2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA		—	—	0.4	V

* $V_{CC} = 5V$, $T_a = 25^\circ C$

I/O capacitance

($T_a = 25^\circ C$, $f = 1MHz$)

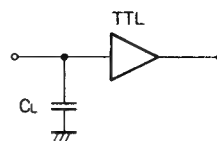
Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics**● AC test conditions** ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)

Item		Conditions
Input pulse high level		$V_{IH} = 2.2V$
Input pulse low level		$V_{IL} = 0.8V$
Input rise time		$t_r = 5ns$
Input fall time		$t_f = 5ns$
Input and output reference level		1.5V
Output load	85L/10L/12L	$C_L^* = 100pF$, 1TTL
	70L	$C_L^* = 30pF$, 1TTL

* C_L includes scope and jig capacitances.



• Read cycle

Item	Symbol	- 70L		- 85L		- 10L		- 12L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time (CE1, CE2)	t _{CO1} , t _{CO2}	—	70	—	85	—	100	—	120	ns
Output hold from address change	t _{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	10	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	0	30	0	30	0	30	0	30	ns

* t_{HZ1} and t_{HZ2} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

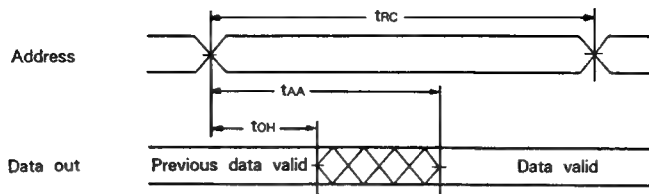
• Write cycle

Item	Symbol	- 70L		- 85L		- 10L		- 12L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

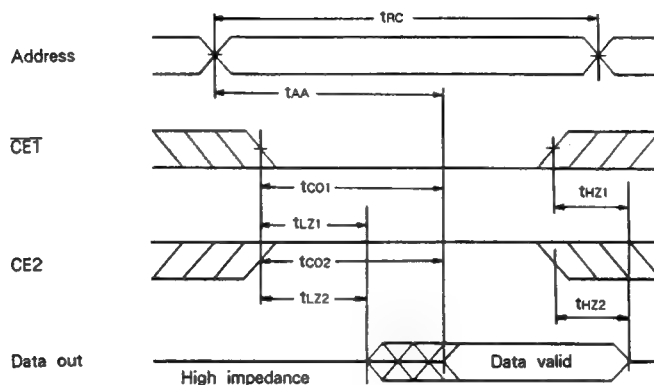
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

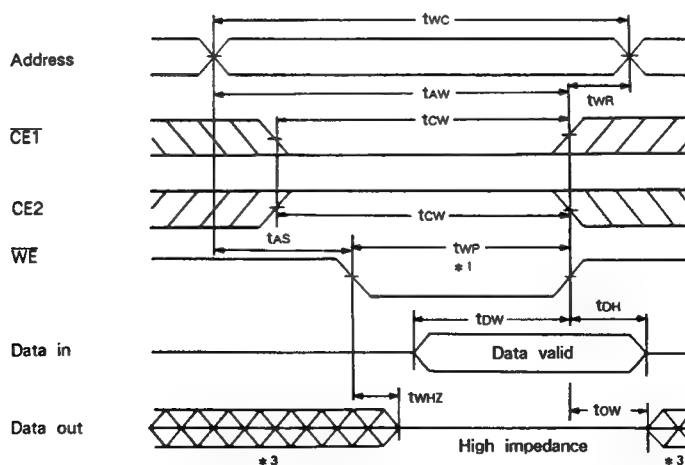
- Read cycle (1) : $\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



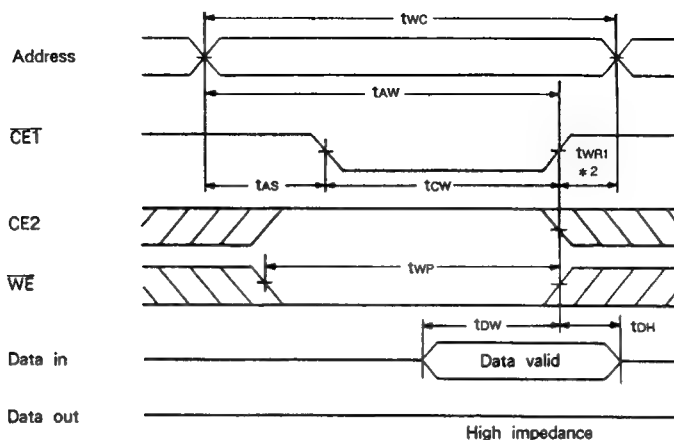
- Read cycle (2) : $\overline{WE} = V_{IH}$



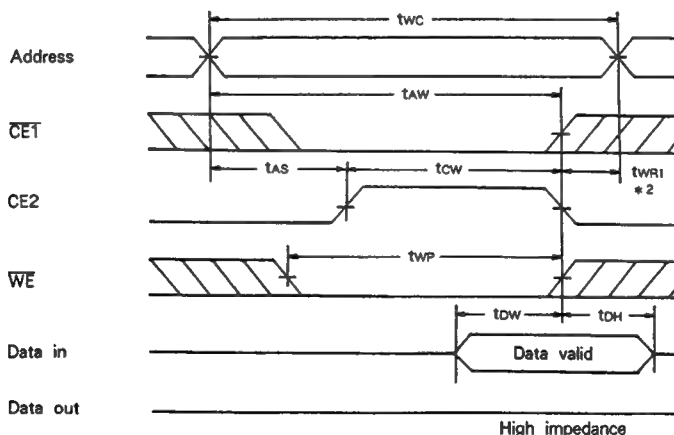
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



- *1. A write occurs during the period of $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ being low and CE2 being high.
- *2. t_{WH1} is measured from the earlier of $\overline{\text{CE1}}$ or $\overline{\text{WE}}$ going high and CE2 going low to the end of write cycle.
- *3. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

(Ta = 0 to 70°C)

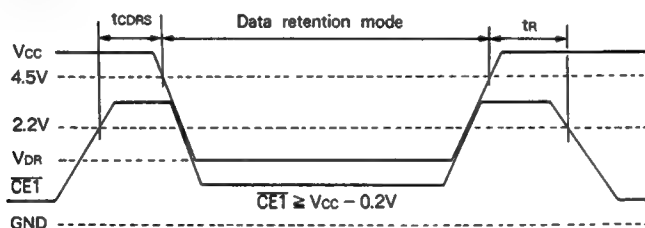
Item	Symbol	Test conditions		- 70L/85L/10L/12L			Unit
				Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1		2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} = 3.0V *1	0 to 70°C	—	—	10	μA
			0 to 40°C	—	—	2	
			25°C	—	0.25	1	
	I _{CCDR2}	V _{CC} = 2.0 to 5.5V *1		—	0.5	25	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t _R			t _{RC} *2	—	—	ns

*1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

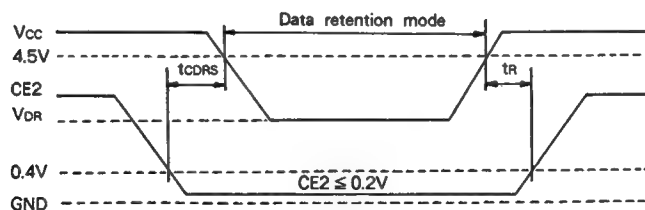
*2. t_{RC}: Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

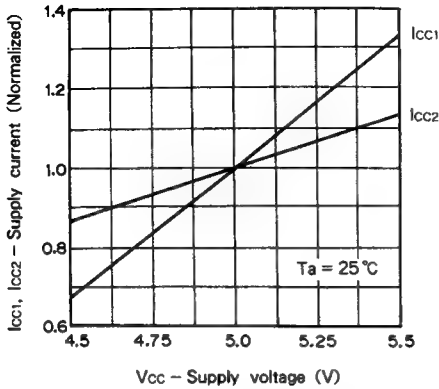


- Low supply voltage data retention waveform (2) ($CE2$ control)

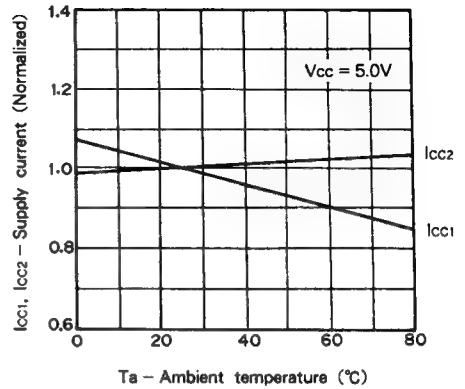


Example of Representative Characteristics

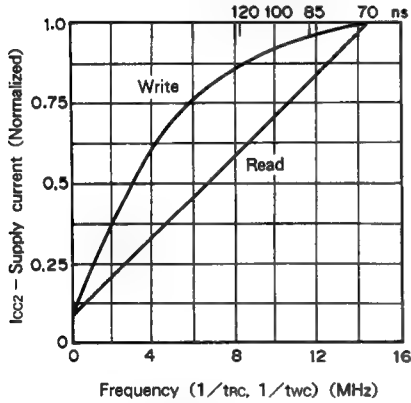
Supply current vs. Supply voltage



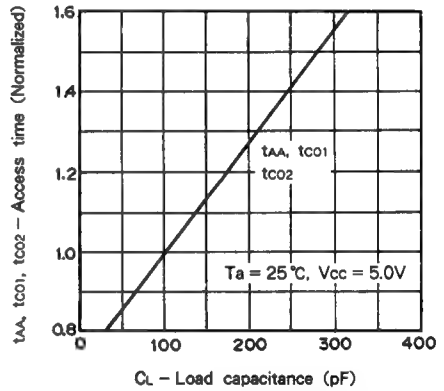
Supply current vs. Ambient temperature



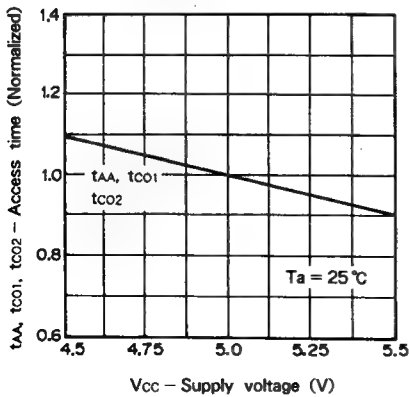
Supply current vs. Frequency



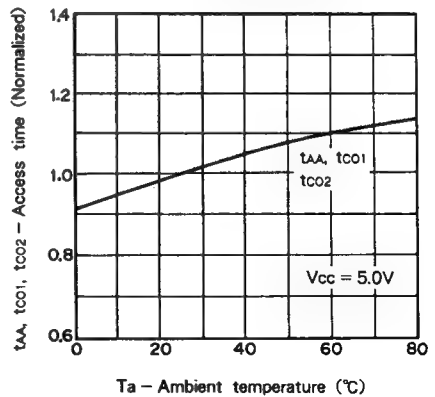
Access time vs. Load capacitance



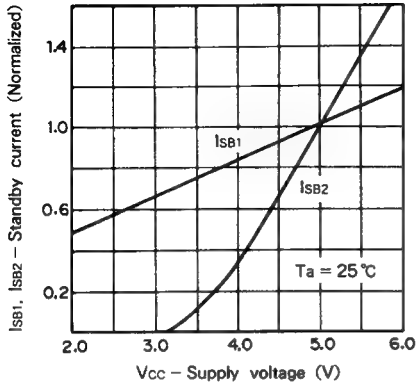
Access time vs. Supply voltage



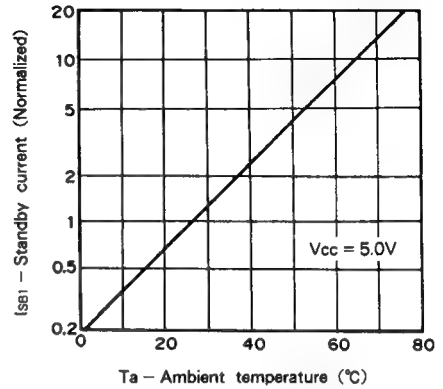
Access time vs. Ambient temperature



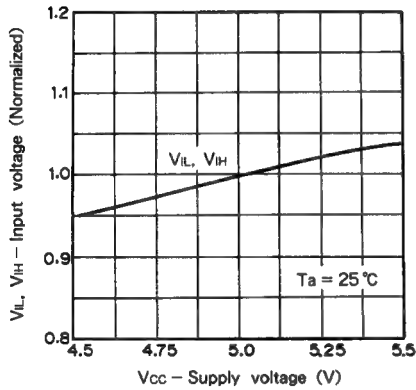
Standby current vs. Supply voltage



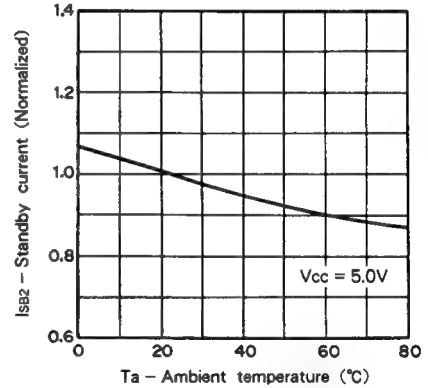
Standby current vs. Ambient temperature



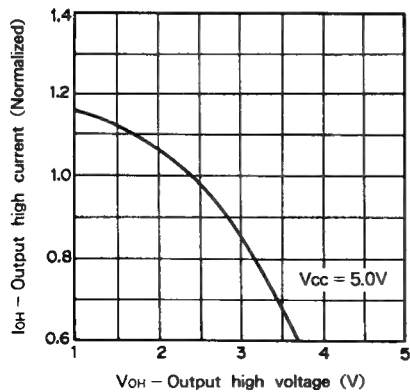
Input voltage level vs. Supply voltage



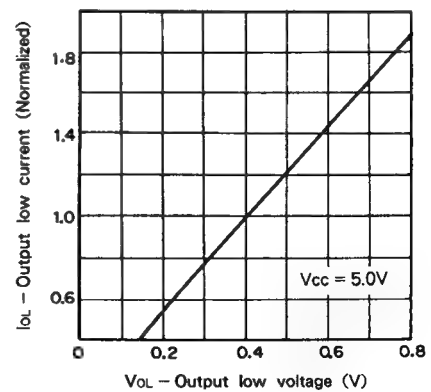
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



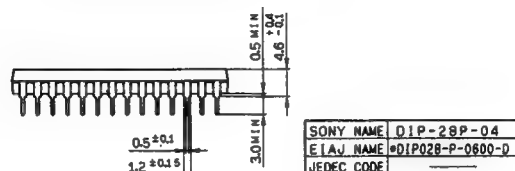
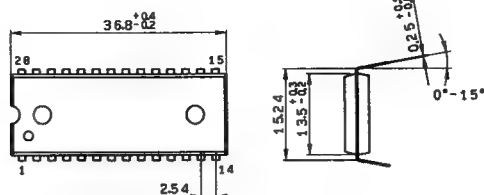
Output low current vs. Output low voltage



Package Outline Unit : mm

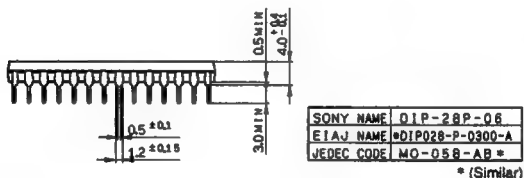
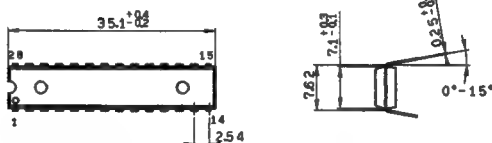
CXK58267AP

28pin DIP (Plastic) 600mil 4.2g



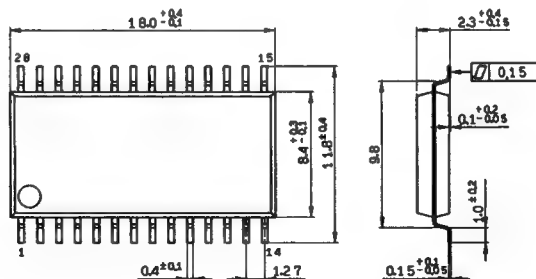
CXK58267ASP

28pin DIP (Plastic) 300mil 2.0g



CXK58267AM

28pin SOP (Plastic) 450mil 0.7g



SONY**CXK59288P/J** -15*/17/20/25**32768-word × 9-bit High Speed CMOS Static RAM * under development****Description**

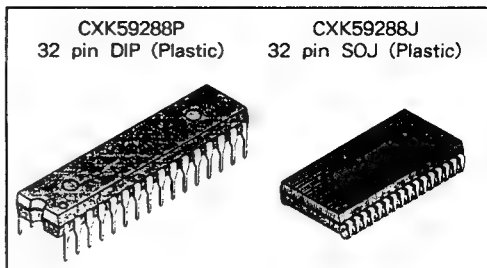
The CXK59288P/J is a high speed CMOS static RAM which consists of 32768-word × 9-bit. It operates at 15ns/17ns/20ns/25ns access time from 5V single power supply.

Features

- High speed, low power consumption :

	Access time (Max.)	Power consumption (Typ., Cycle=Min.)
CXK59288P/J-15	15ns	500mW
CXK59288P/J-17	17ns	450mW
CXK59288P/J-20	20ns	400mW
CXK59288P/J-25	25ns	350mW

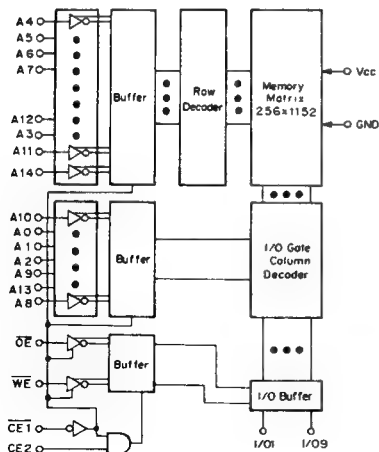
- Single +5V power supply :
 - 15/17 5V ± 5 %
 - 20/25 5V ± 10 %
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible all inputs and outputs.
- Available in 32 pin 300mil DIP, 300mil SOJ package.

**Function**

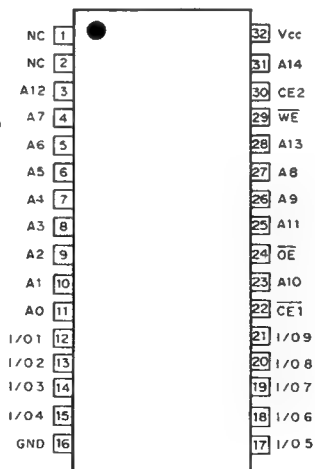
32768-word × 9-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration**

(Top View)

**Pin Description**

Symbol	Description
A0 to A14	Address input
I/O1 to I/O9	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

(Ta = 25 °C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.**Truth Table**

$\overline{CE1}$	CE2	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O9	V _{CC} Current
H	x	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	L	x	x	Not selected	High Z	I _{CC1} , I _{CC2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	x	L	Write	Data in	I _{CC1} , I _{CC2}

x : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to + 70 °C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.75	5.0	5.25	V
		4.5	5.0	5.5	
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics (V_{CC} = 5V ± 10%*, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.**	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	-1	μA
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL}	-1	—	-1	μA
Operating power supply current	I _{CC1}	CE1 = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	—	—	
Average operating current	I _{CC2}	Cycle = Min, Duty = 100%, I _{OUT} = 0mA	-15	—	100	mA
			-17	—	90	
			-20	—	80	
			-25	—	70	
Standby current	I _{SB1}	CE1 ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	1	mA
	I _{SB2}	CE1 = V _{IH} , V _{IN} = V _{IH} /V _{IL} , Cycle = Min.	—	20	30	
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V ± 5% for CXK59288P/J-15/17** V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

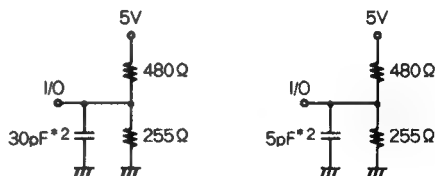
• AC test conditions

(V_{CC} = 5V ± 10%*, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 3ns
Input fall time	t _f = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)

Output Load (2)*3

*1 V_{CC} = 5V ± 5% for CXK59288P/J-15/17

*2 including scope and jig capacitance

*3 for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	- 15		- 17		- 20		- 25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	15	—	17	—	20	—	25	—	ns
Address access time	t _{AA}	—	15	—	17	—	20	—	25	ns
Chip enable access time (CE1)	t _{CO1}	—	15	—	17	—	20	—	25	ns
Chip enable access time (CE2)	t _{CO2}	—	8	—	9	—	10	—	12	ns
Output enable to output valid	t _{OE}	—	8	—	9	—	10	—	12	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LE1} *, t _{LE2} *	3	—	3	—	3	—	3	—	ns
Output enable to output in low Z (OE)	t _{OLZ} *, t _{OHZ1} *	2	—	2	—	2	—	2	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ2} *	—	8	—	8	—	9	—	10	ns
Output disable to output in high Z (OE)	t _{OHZ} *	—	7	—	7	—	8	—	9	ns
Chip enable to power up time (CE1)	t _{PU}	0	—	0	—	0	—	0	—	ns
Chip disable to power down time (CE1)	t _{PD}	—	15	—	17	—	20	—	25	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

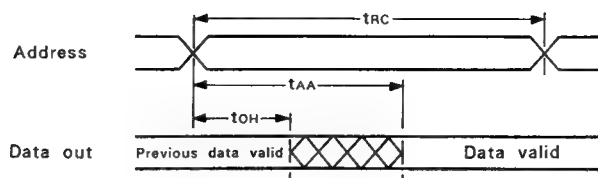
• Write cycle

Item	Symbol	- 15		- 17		- 20		- 25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	15	—	17	—	20	—	25	—	ns
Address valid to end of write	t _{AW}	11	—	12	—	13	—	15	—	ns
Chip enable to end of write	t _{CW}	12	—	13	—	14	—	16	—	ns
Data to write time overlap	t _{DW}	9	—	10	—	11	—	12	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	10	—	11	—	13	—	15	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	3	—	3	—	3	—	3	—	ns
Write to output in high Z	t _{WHZ} *	0	8	0	8	0	9	0	10	ns

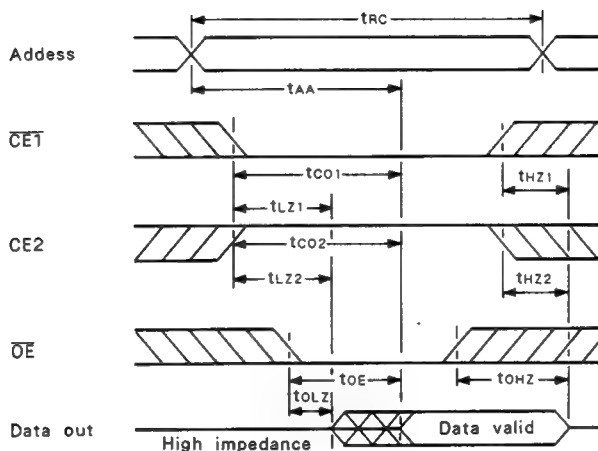
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

Timing Waveform

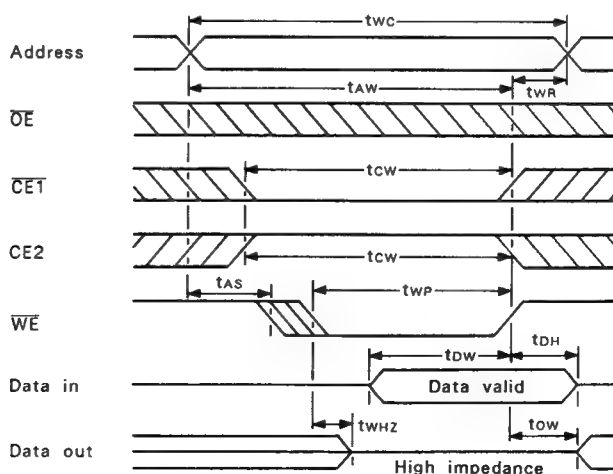
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



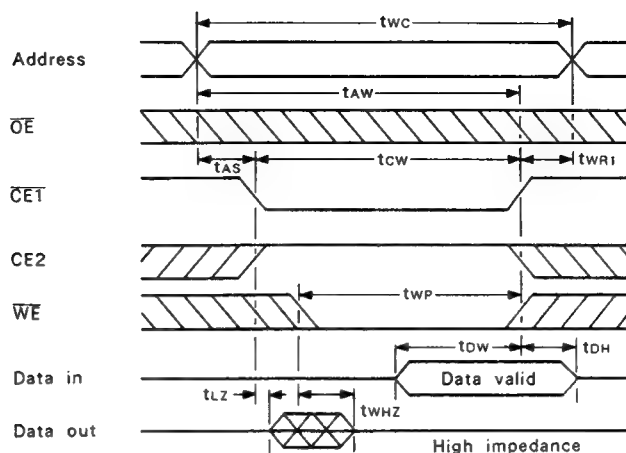
- Read cycle (2) : $\overline{WE} = V_{IH}$



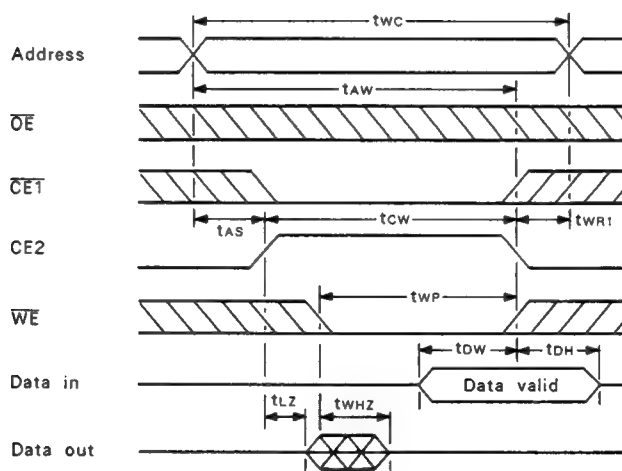
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE1}}$ control



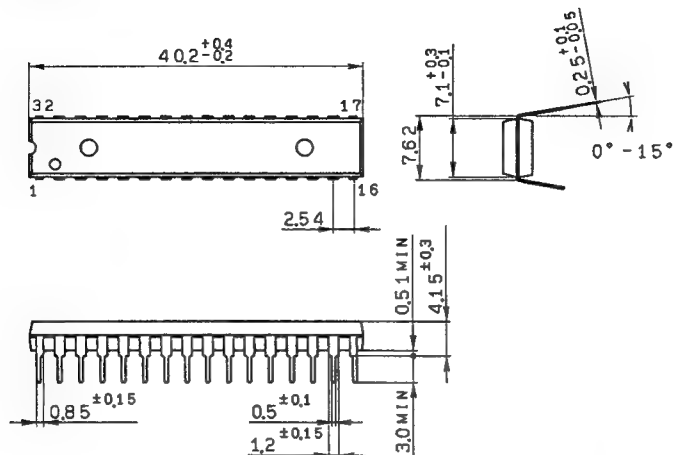
• Write cycle (3) : $\overline{\text{CE2}}$ control



* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

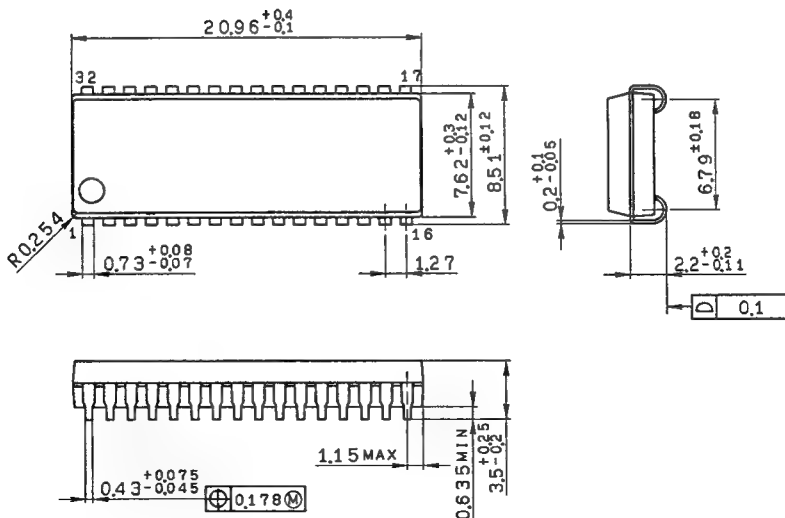
Package Outline Unit : mm

CXK59288P 32pin DIP (Plastic) 300mil



SONY NAME	DIP-32P-03
EIAJ NAME	*DIP032-P-0300-A
JEDEC CODE	

CXK59288J 32pin SOJ (Plastic) 300mil



SONY NAME	SOJ-32P-02
EIAJ NAME	*SOJ032-P-0300-A
JEDEC CODE	MO-077-AC

SONY**CXK59289P/M*** -20/25**32,768-word × 9-bit High Speed CMOS Static RAM * under development****Description**

The CXK59289P/M is a high speed CMOS static RAM which consists of 32,768-word × 9-bit. It operates at 20ns/25ns access time from 5V single power supply.

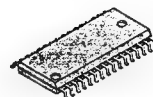
Features

- High speed, low power consumption :

	Access time	Power consumption
	(Max.)	(Typ., Cycle=Min.)
CXK59289P/M-20	20ns	400mW
CXK59289P/M-25	25ns	350mW
- Single + 5V power supply : $5V \pm 10\%$
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible all inputs and outputs.
- Available in 32 pin 300mil DIP, 450mil SOP package.

CXK59289P
32 pin DIP (Plastic)

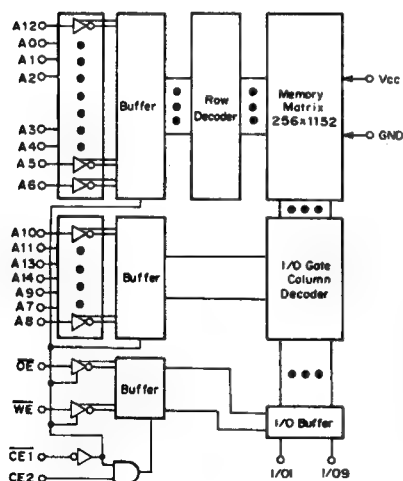
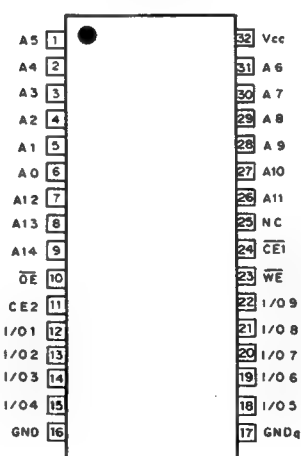
CXK59289M
32 pin SOP (Plastic)

**Function**

32,768-word × 9-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration**
(Top View)**Pin Description**

Symbol	Description
A0 to A14	Address input
I/O1 to I/O9	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V power supply
GND, GNDq	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5* to +7.0	V
Input voltage	V _{IN}	-0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	-0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature * time	T _{solder}	260 * 10	°C * sec

* V_{CC}, V_{IN}, V_{I/O} = -3.5V Min. for pulse width less than 20ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O1 to I/O9	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	L	X	X	Not selected	High Z	I _{CC1} , I _{CC2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

* V_{IL} = -3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	1	μA
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL}	-1	—	1	μA
Operating power supply current	I _{CC1}	CE1 = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	—	—	
Average operating current	I _{CC2}	Cycle = Min, Duty = 100%, I _{OUT} = 0mA	-20	80	120	mA
			-25	70	120	
Standby current	I _{SB1}	CE1 ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	1	mA
	I _{SB2}	CE1 = V _{IH} , V _{IN} = V _{IH} /V _{IL} , Cycle = Min.	—	20	30	
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

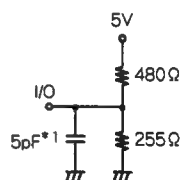
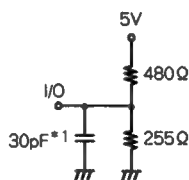
• AC test conditions

(V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 3ns
Input fall time	t _f = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)

Output Load (2) *2



*1 including scope and jig capacitance

*2 for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	- 20		- 25		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	20	—	25	—	ns
Address access time	t _{AA}	—	20	—	25	ns
Chip enable access time (CE1)	t _{CO1}	—	20	—	25	ns
Chip enable access time (CE2)	t _{CO2}	—	10	—	12	ns
Output enable to output valid	t _{OE}	—	10	—	12	ns
Output hold from address change	t _{OH}	5	—	5	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} *, t _{LZ2} *	3	—	3	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ} *	2	—	2	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	—	9	—	10	ns
Output disable to output in high Z (\overline{OE})	t _{OHZ} *	—	8	—	9	ns
Chip enable to power up time ($\overline{CE1}$)	t _{PU}	0	—	0	—	ns
Chip disable to power down time ($\overline{CE1}$)	t _{PD}	—	20	—	25	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

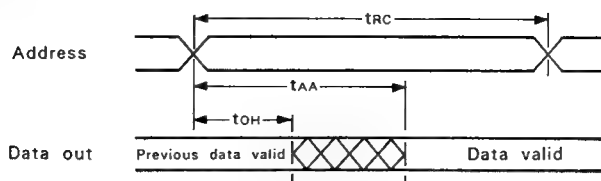
• Write cycle

Item	Symbol	- 20		- 25		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	20	—	25	—	ns
Address valid to end of write	t _{AW}	13	—	15	—	ns
Chip enable to end of write	t _{CW}	14	—	16	—	ns
Data to write time overlap	t _{DW}	11	—	12	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	13	—	15	—	ns
Address set up time	t _{AS}	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t _{WR1}	0	—	0	—	ns
Output active from end of write	t _{OW} *	3	—	3	—	ns
Write to output in high Z	t _{WHZ} *	—	9	—	10	ns

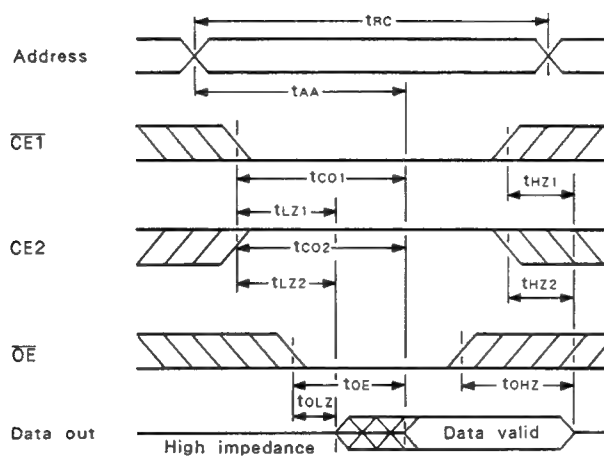
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

Timing Waveform

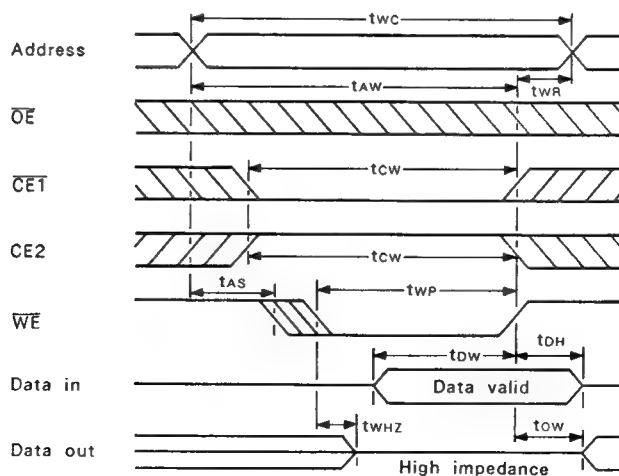
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



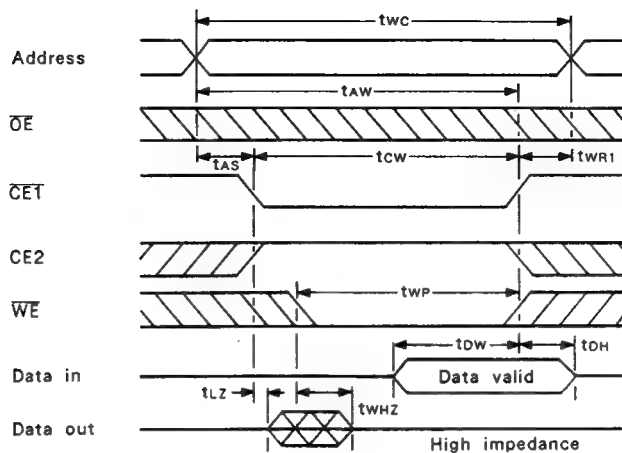
- Read cycle (2) : $\overline{WE} = V_{IH}$



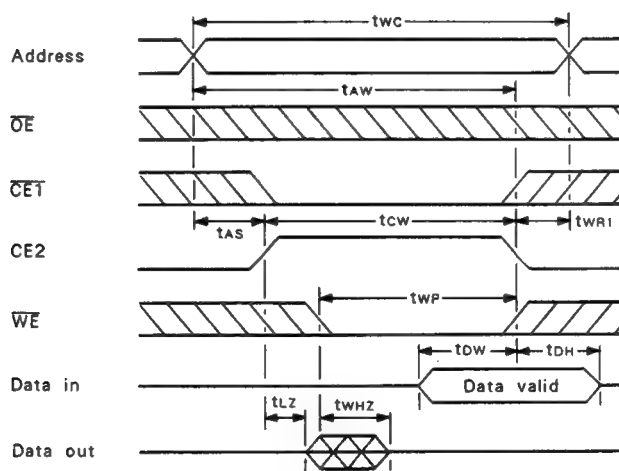
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : $\overline{CE2}$ control

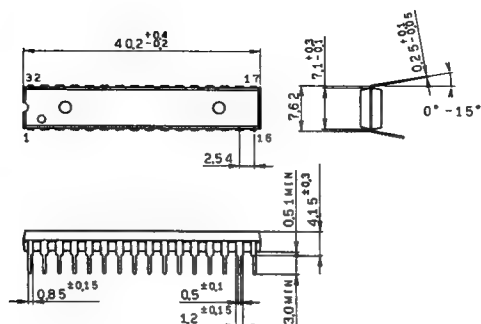


* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

CXK59289P

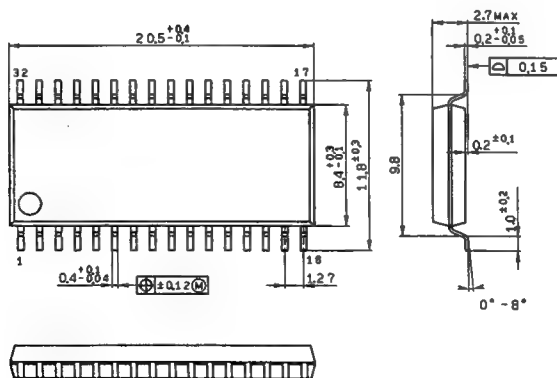
32pin DIP (Plastic) 300mil



SONY NAME	DIP-32P-03
EIAJ NAME	*DIP032-P-0300-A
JEDEC CODE	

CXK59289M

32pin SOP (Plastic) 450mil



SONY NAME	SOP-32P-L03
EIAJ NAME	*SOP032-P-0450-B
JEDEC CODE	

SONY

CXK59290M/TM -70L/10L/12L

32768-word × 9-bit High Speed CMOS Static RAM (SOP is under developing)

Description

The CXK59290M/TM is a 294912 bits high speed CMOS static RAM organized as 32768 words by 9 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time: (Access time)
CXK59290M/TM-70L 70ns (Max.)
CXK59290M/TM-10L 100ns (Max.)
CXK59290M/TM-12L 120ns (Max.)
- Low power operation: Standby/Operation
CXK59290M/TM-70L, 10L, 12L: 2.5μW (Typ.)/15mW (Typ.)
- Single +5V supply: +5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 32 pin 450mil SOP and 32 pin 8mm × 20mm TSOP (EIAJ Standard)

CXK59290M
32 pin SOP (Plastic)



CXK59290TM
32 pin TSOP (Plastic)



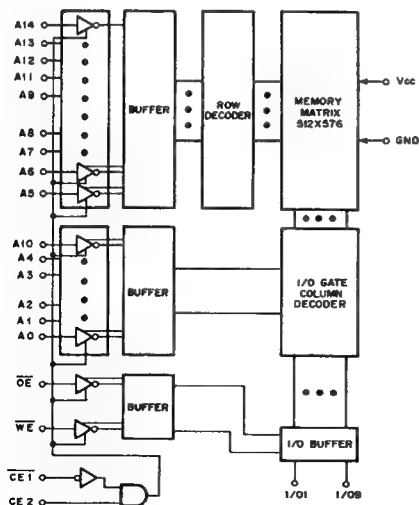
Function

32768-word × 9-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram

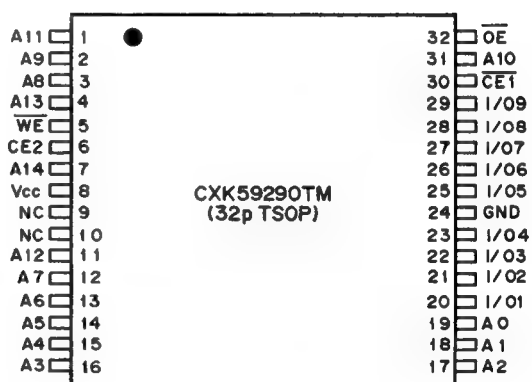
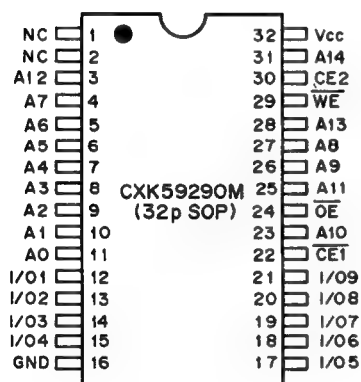


Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O9	Data input/output
$\overline{CE}1$, $\overline{CE}2$	Chip enable 1, 2 input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Pin Configuration

(Top View)



Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature	T _{solder}	M	°C · sec
		TM	
		260 · 10	
		235 · 10	

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O9	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions		Min.	Typ. *	Max.	Unit
Input leakage current	I _I	V _{IN} =GND to V _{CC}		-0.5	—	0.5	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} , V _{IO} =GND to V _{CC}		-0.5	—	0.5	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} , I _{OUT} =0mA V _{IN} =V _{IH} or V _{IL}		—	25	50	mA
		CE1 ≤ 0.2V, CE2 ≥ V _{CC} -0.2V V _{IN} ≤ 0.2V or ≥ V _{CC} -0.2V		—	23	45	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	70L	—	—	70	mA
			10L	—	—	70	
			12L	—	—	70	
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} -0.2V CE2 ≥ V _{CC} -0.2V	0 to +70 °C	—	—	25	μA
			0 to +40 °C	—	—	5	
			25 °C	—	0.5	2	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}		—	0.4	2	mA
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

(T_a=25 °C, f=1MHz)

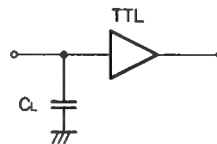
Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{IO}	V _{IO} =0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions (V_{CC}=5V ± 10%, T_a=0 to +70 °C)

Item		Conditions
Input pulse high level		V _{IH} =2.2V
Input pulse low level		V _{IL} =0.8V
Input rise time		t _r =5ns
Input fall time		t _f =5ns
Input and output reference level		1.5V
Output load conditions	10L/12L	C _L *=100pF, 1TTL
	70L	C _L *=30pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	-70L		-10L		-12L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	100	—	120	ns
Chip enable access time ($\overline{\text{CE1}}$)	t _{CO1}	—	70	—	100	—	120	ns
Chip enable access time (CE2)	t _{CO2}	—	70	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	50	—	60	ns
Output hold from address change	t _{OH}	5	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{\text{CE1}}$, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{\text{CE1}}$, CE2)	t _{HZ1} , t _{HZ2} *	0	30	0	30	0	30	ns
Chip disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to as output voltage levels.

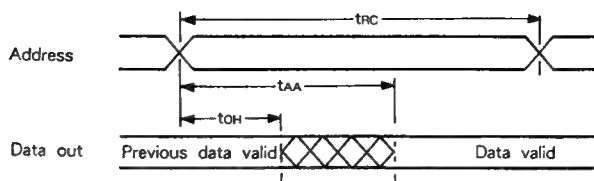
• Write cycle

Item	Symbol	-70L		-10L		-12L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	60	—	70	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{CE1}}$, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	ns

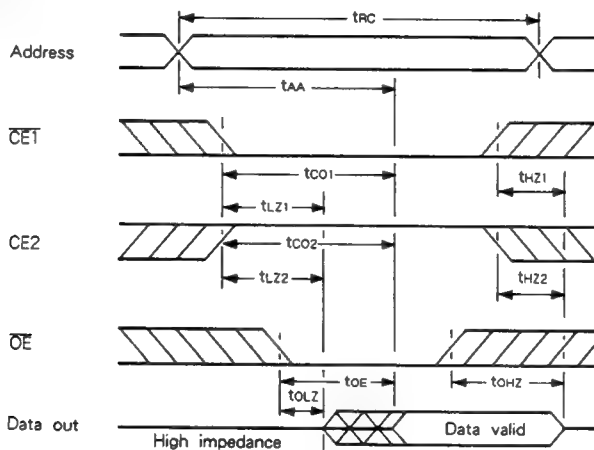
* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to as output voltage levels.

Timing Waveform

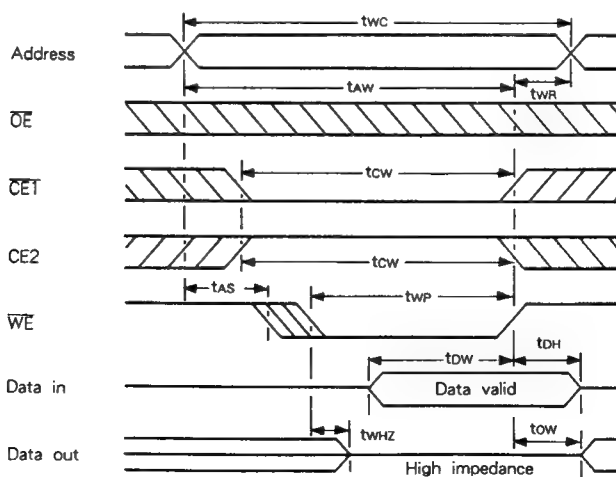
- Read cycle (1) : $\overline{CE1}=\overline{OE}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



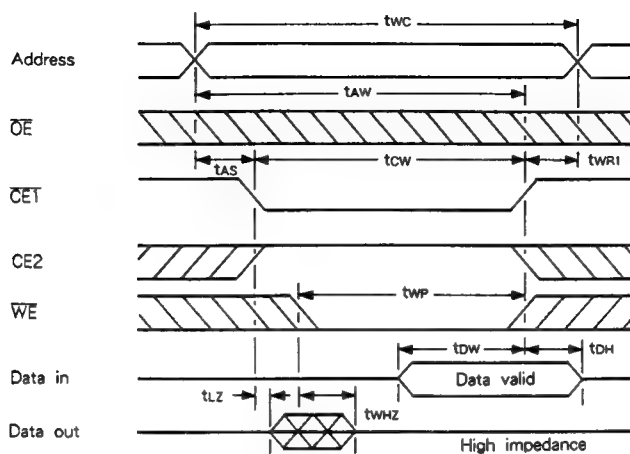
- Read cycle (2) : $\overline{WE}=V_{IH}$



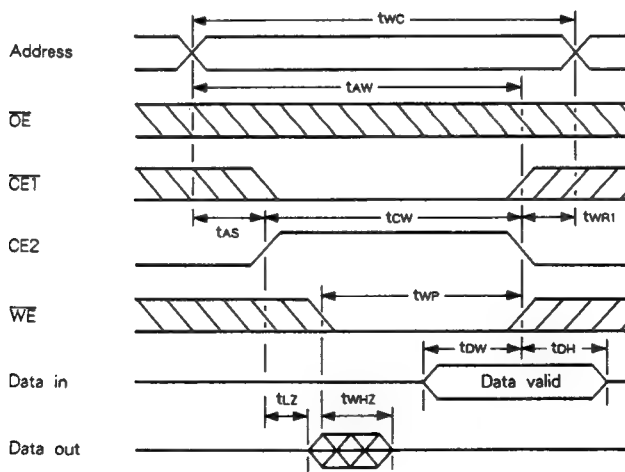
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : $\overline{\text{CE2}}$ control



* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

(Ta=0 to +70°C)

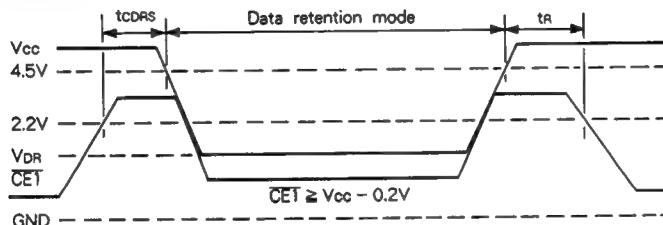
Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V _{DR}	*1		2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V *1	0 to +70°C	—	—	10	μA
			0 to +40°C	—	—	2	
			25°C	—	0.25	1	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V *1		—	0.5 *3	25	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention		0	—	—	ns
Recovery time	t _R	mode		t _{RC} *2	—	—	ns

*1. $\overline{CE1} \geq V_{CC}-0.2V$, $CE2 \geq V_{CC}-0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

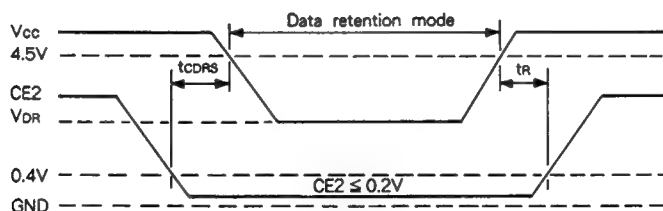
*2. t_{RC} : Read cycle time

*3. V_{CC}=5V, Ta=25°C

• Low supply voltage data retention waveform (1) : $\overline{CE1}$ control

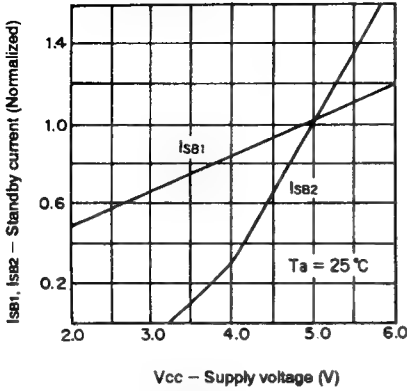


• Low supply voltage data retention waveform (2) : $CE2$ control

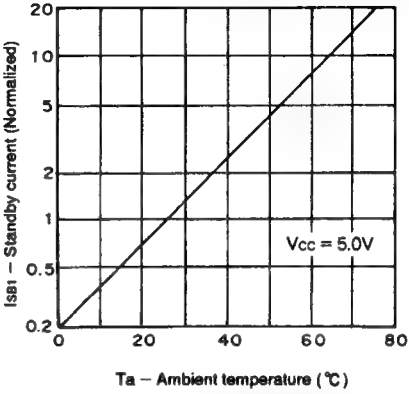


Example of Representative Characteristics

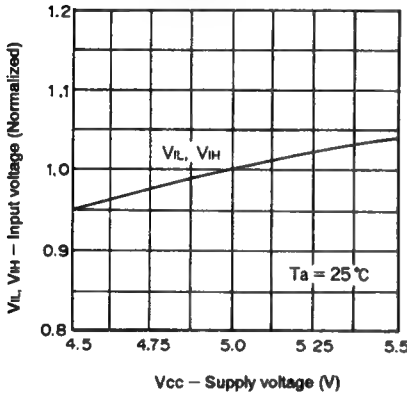
Standby current vs. Supply voltage



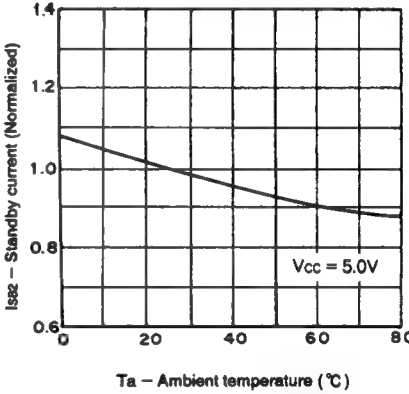
Standby current vs. Ambient temperature



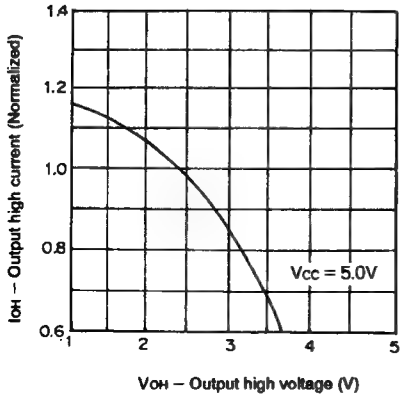
Input voltage level vs. Supply voltage



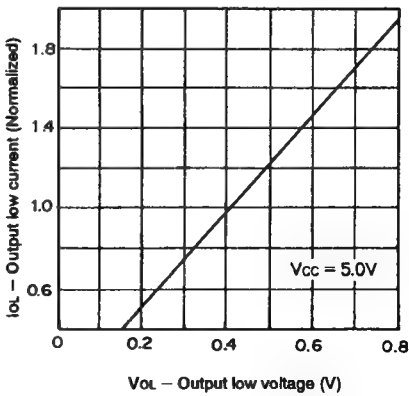
Standby current vs. Ambient temperature



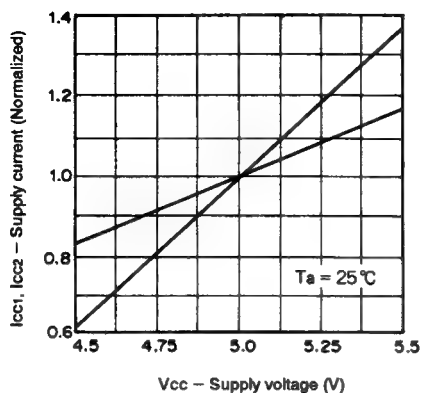
Output high current vs. Output high voltage



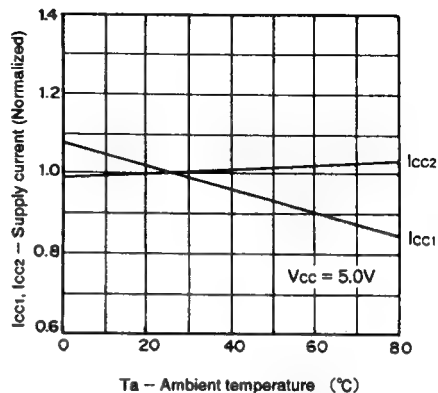
Output low current vs. Output low voltage



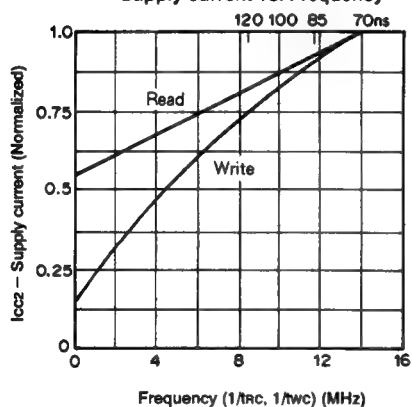
Supply current vs. Supply voltage



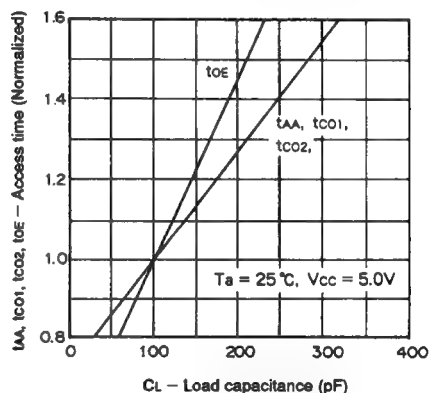
Supply current vs. Ambient temperature



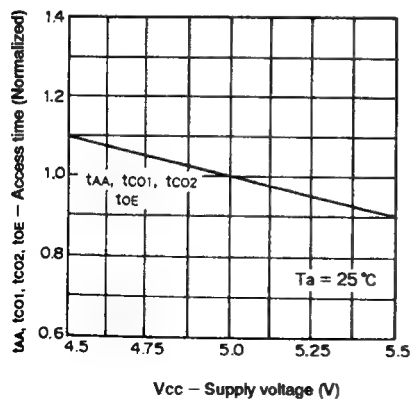
Supply current vs. Frequency



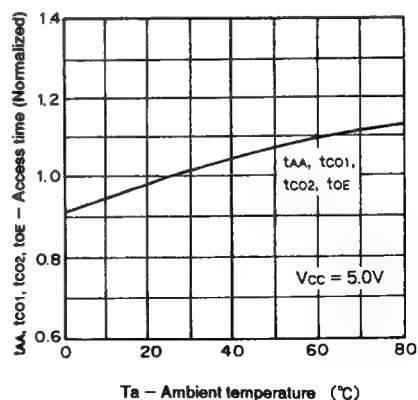
Access time vs. Load capacitance



Access time vs. Supply voltage



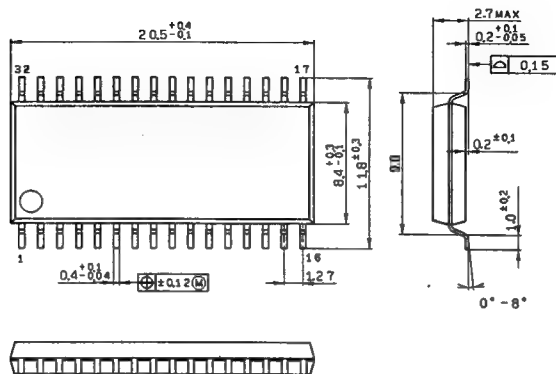
Access time vs. Ambient temperature



Package Outline Unit : mm

CXK59290M

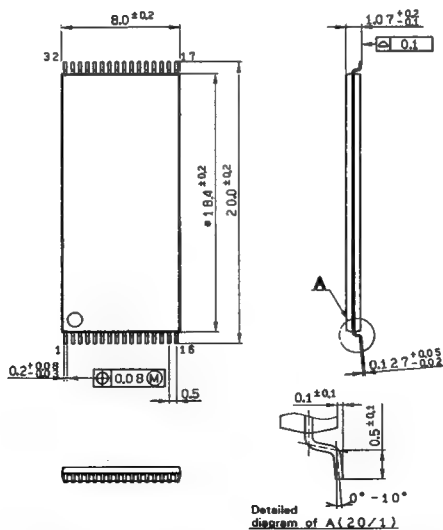
32pin SOP (Plastic) 450mil



SONY NAME	SOP-32P-L03
EIAJ NAME	*SOP032-P-0450-B
JEDEC CODE	

CXK59290TM

32pin TSOP (Plastic)



Note) Dimensions marked with *
does not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	

CXK581000P/M -10L/12L/15L
-10LL/12LL/15LL

131072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131, 072 words by 8 bits. Operating on a single 5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

Features

- Fast access time : (Access time)
 CXK581000P/M-10L/10LL 100ns (Max.)
 CXK581000P/M-12L/12LL 120ns (Max.)
 CXK581000P/M-15L/15LL 150ns (Max.)
- Low power consumption operation :

	Standby	/DC operation
CXK581000P/M-10L, 12L, 15L ;	10 μ W (Typ.)	/35mW (Typ.)
10LL, 12LL, 15LL ;	3.5 μ W (Typ.)	/35mW (Typ.)
- Single +5V supply : +5V \pm 10%
- Fully static memory \cdots No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581000P 600mil 32 pin DIP package
 CXK581000M 525mil 32 pin SOP package

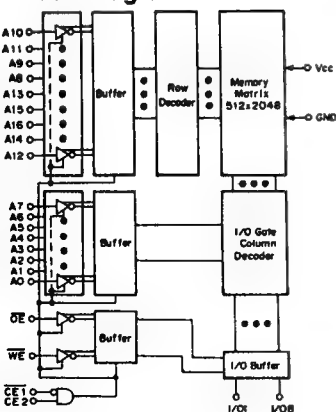
Functions

131,072 word × 8 bit static RAM

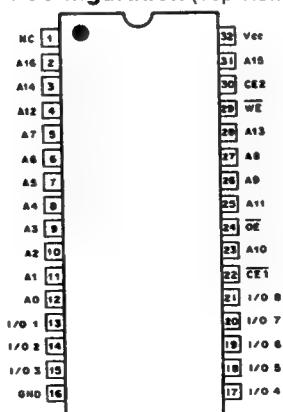
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{\text{CE}}1, \text{CE}2$	Chip enable 1, 2 input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{OE}}$	Output enable input
V_{CC}	Power supply
GND	Ground
NC	No connection

E89322C06 - ST

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to +7.0	V
Input voltage	V _{IN}	- 0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{IO}	- 0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK581000P	1.0
		CXK581000M	0.7
Operating temperature	T _{OPR}	0 to +70	°C
Storage temperature	T _{STG}	- 55 to +150	°C
Soldering temperature	T _{SDR}	260•10	°C • sec

* V_{IN}, V_{IO} = - 3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O pin	V _{CC} current
H	x	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
x	L	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	x	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

x : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	- 0.3 *	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions		- 10L/12L/15L			- 10LL/12LL/15LL			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		- 1	—	1	- 1	—	1	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} V _{IO} =GND to V _{CC}		- 1	—	1	- 1	—	1	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA		—	7	15	—	7	15	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty=100% I _{OUT} =0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} - 0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} - 0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V CE1 ≥ V _{CC} - 0.2V or CE2 ≥ V _{CC} - 0.2V	0 to 70 °C	—	—	100	—	—	20	μA
			0 to 40 °C	—	—	20	—	—	4	
			+25 °C	—	2	8	—	0.7	2	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	0.6	3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} = - 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

(T_a=25 °C, f=1MHz)

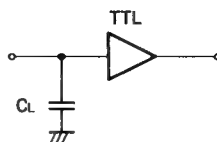
Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	6	pF
I/O capacitance	C _{I/O}	V _{IO} =0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics**• AC test conditions** ($V_{CC}=5V \pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$)

Item	Conditions
Input pulse high level	$V_{IH}=2.2V$
Input pulse low level	$V_{IL}=0.8V$
Input rise time	$t_r=5ns$
Input fall time	$t_f=5ns$
Input and output reference level	1.5V
Output load conditions	$C_L^* = 100pF$, 1TTL

* C_L includes scope and jig capacitances.

• Test circuit

• Read cycle (\overline{WE} ="H")

Item	Symbol	- 10L/10LL		- 12L/12LL		- 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	100	—	120	—	150	—	ns
Address access time	t _{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	100	—	120	—	150	ns
Chip enable access time (CE2)	t _{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t _{OE}	—	50	—	60	—	70	ns
Output hold from address change	t _{OH}	15	—	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t _{HZ1} *, t _{HZ2} *	—	35	—	40	—	50	ns
Output disable to output in high Z (\overline{OE})	t _{OHZ} *	—	35	—	40	—	50	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

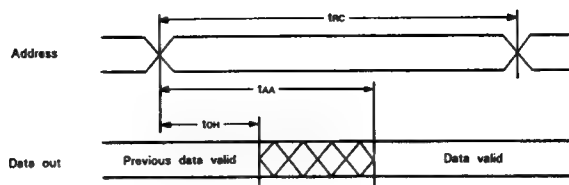
• Write cycle

Item	Symbol	- 10L/10LL		- 12L/12LL		- 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t _{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t _{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t _{DW}	40	—	50	—	60	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	70	—	80	—	90	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	—	30	—	30	—	30	ns

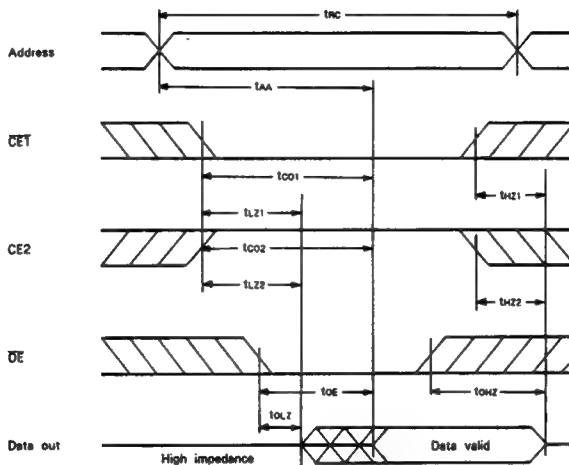
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

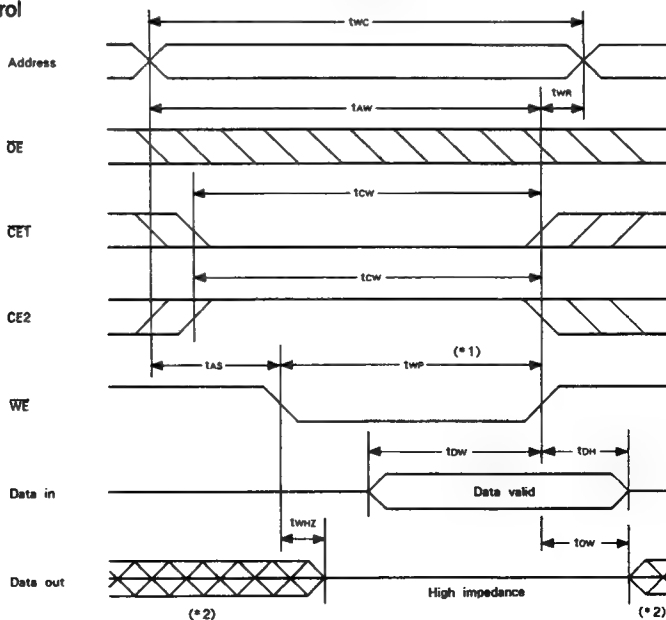
- Read cycle (1) : $\overline{CE1}=\overline{OE}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



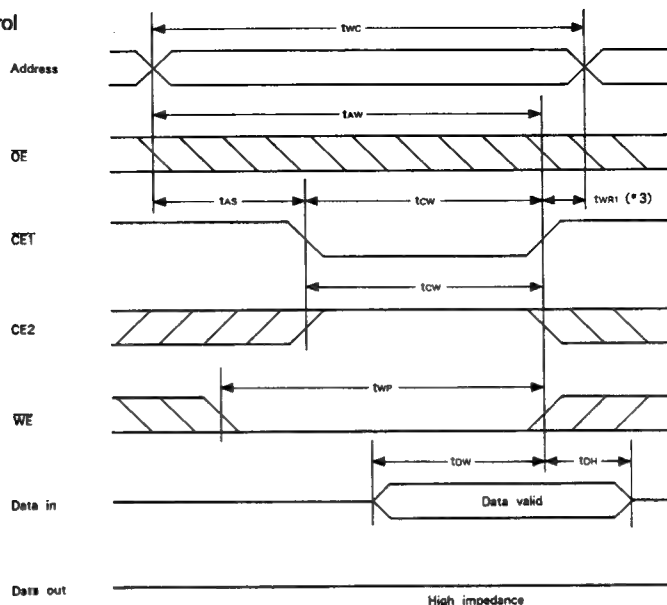
- Read cycle (2) : $\overline{WE}=V_{IH}$



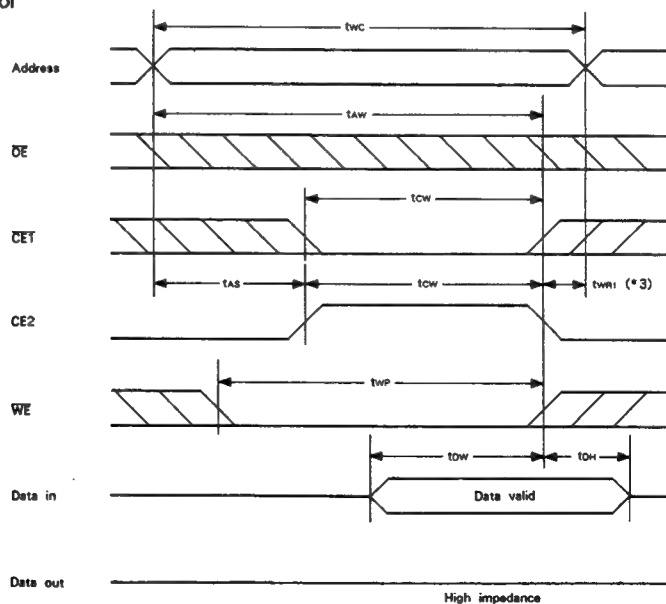
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : $\overline{CE2}$ control



Note)

- * 1. Write is executed when both $\overline{CE1}$ and \overline{WE} are at low and $\overline{CE2}$ is at high simultaneously.
- * 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- * 3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of $\overline{CE2}$, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

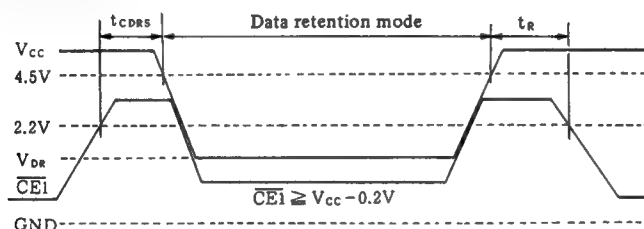
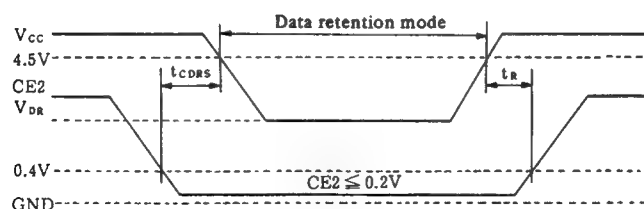
(Ta=0 to 70 °C)

Item	Symbol	Test conditions		- 10L/12L/15L			- 10LL/12LL/15LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V *1	0 to 70 °C	—	—	50	—	—	12	μA
			0 to 40 °C	—	—	10	—	—	2.4	
			+25 °C	—	1	4	—	0.4	1.2	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V *1		—	2	100	—	0.7	20	mA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t _R			t _{RC} *2	—	—	t _{RC} *2	—	—	ns

Note)

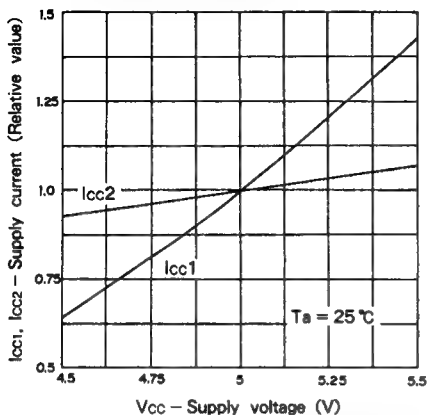
*1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)*2. t_{RC} : Read cycle time

Data retention waveform

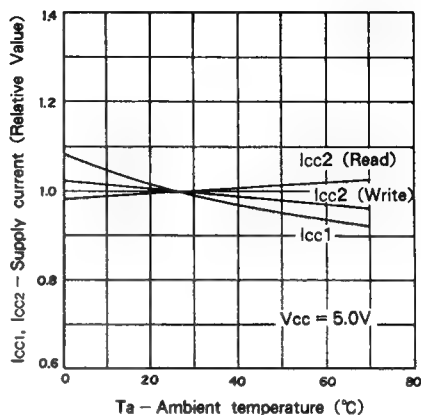
• Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)• Low supply voltage data retention waveform (2) ($CE2$ control)

Example of Representative Characteristics

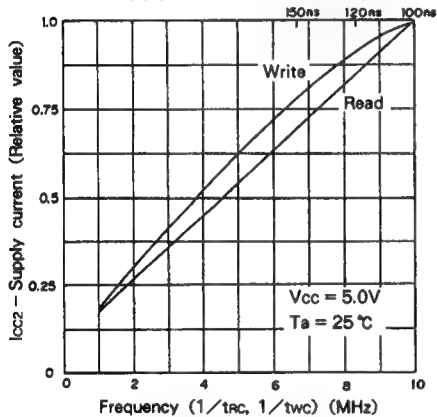
Supply current vs. Supply voltage



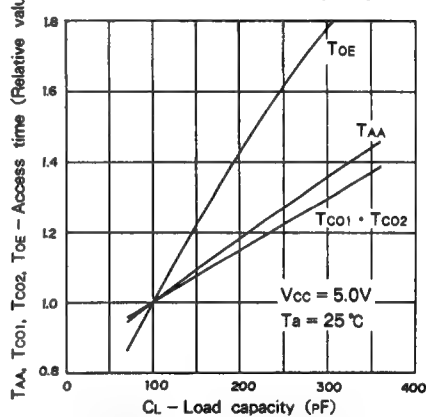
Supply current vs. Ambient temperature



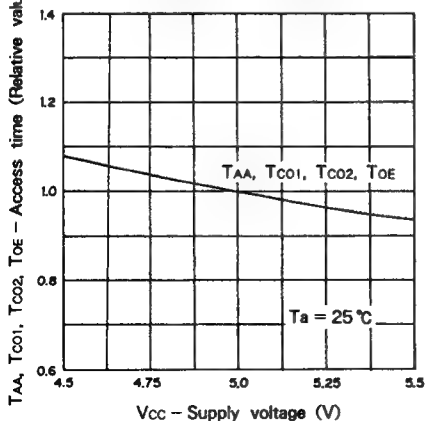
Supply current vs. Frequency



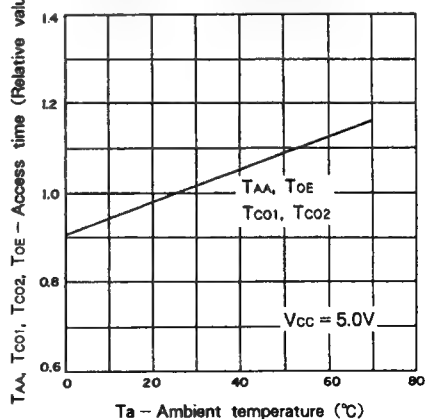
Access time vs. Load capacity



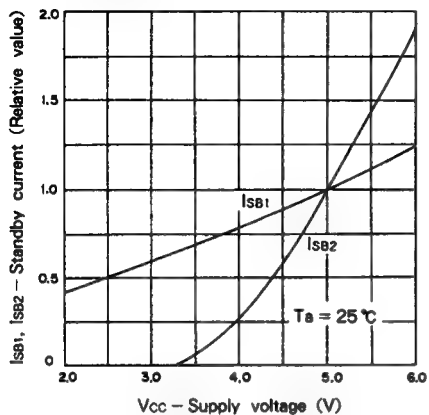
Access time vs. Supply voltage



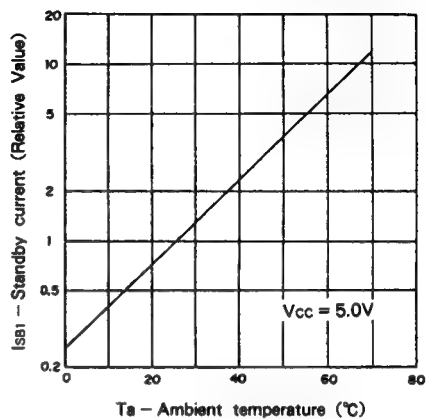
Access time vs. Ambient temperature



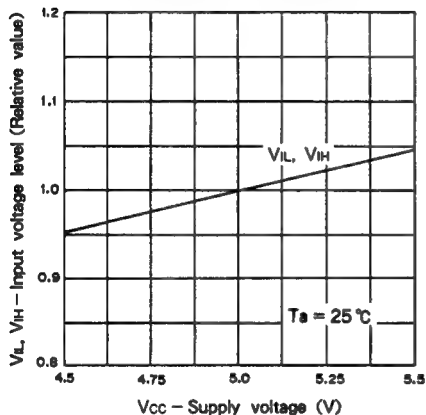
Standby current vs. Supply voltage



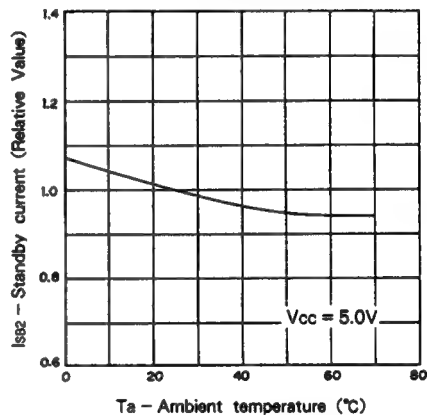
Standby current vs. Ambient temperature



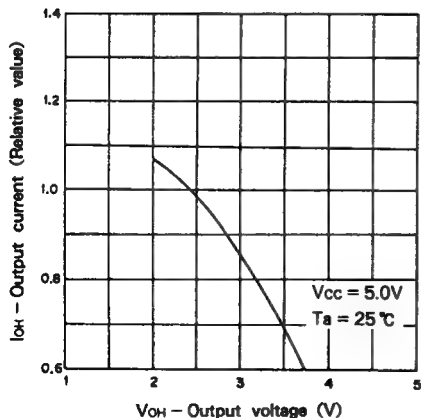
Input voltage level vs. Supply voltage



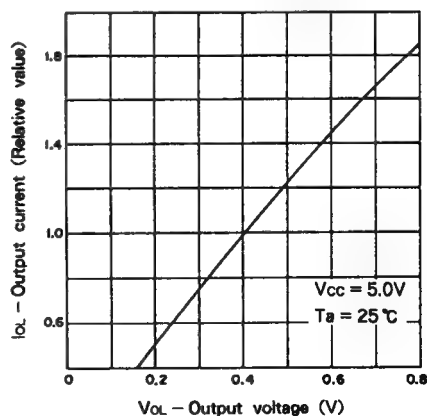
Standby current vs. Ambient temperature



Output current vs. Output voltage

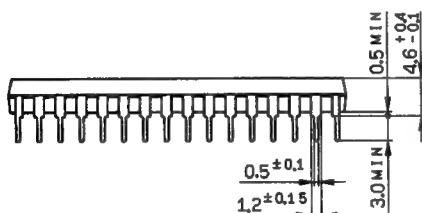
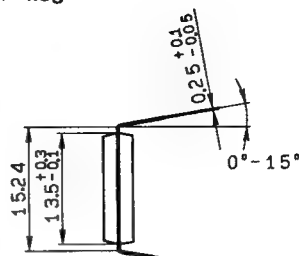
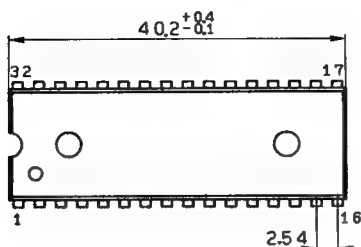


Output current vs. Output voltage



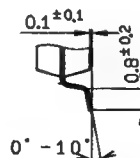
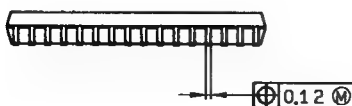
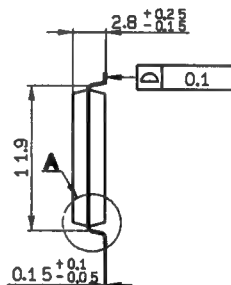
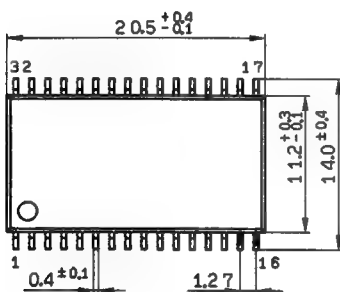
Package Outline Unit : mm

CXK581000P 32Pin DIP (Plastic) 600mil 4.5g



SONY NAME	DIP-32P-01
EIAJ NAME	#DIP032-P-0600-A
JEDEC CODE	

CXK581000M 32Pin SOP (Plastic) 525mil 1.2g



Detailed diagram of A

SONY NAME	SOP-32P-L02
EIAJ NAME	#SOP032-P-0525-A
JEDEC CODE	

SONY® CXK581000P/M -10LX/12LX/15LX/ 10LLX/12LLX/15LLX

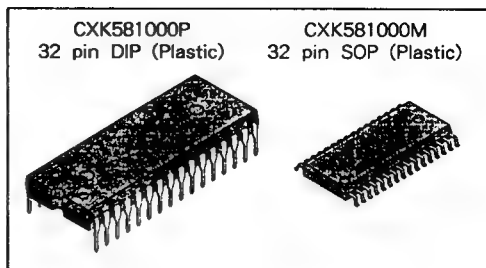
131072-word × 8-bit High Speed CMOS Static RAM

Description

The CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131072 words by 8 bits. Operating on a single 5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

Features

- Extended operating temperature range
(-25°C to +85°C)
- Fast access time (Access time)
CXK581000P/M-10LX/10LLX 100ns (Max.)
CXK581000P/M-12LX/12LLX 120ns (Max.)
CXK581000P/M-15LX/15LLX 150ns (Max.)
- Low power consumption operation
Standby/DC operation
CXK581000P/M-10LX, 12LX, 15LX 10 μW(Typ.)/35mW(Typ.)
CXK581000P/M-10LLX, 12LLX, 15LLX 3.5 μW(Typ.)/35mW(Typ.)
- Single +5V power supply: +5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three state output.
- Directly TTL compatible: All inputs and outputs.
- Low voltage data retention: 2.2V (Min.)
- CXK581000P 600mil 32 pin DIP package
- CXK581000M 525mil 32 pin SOP package



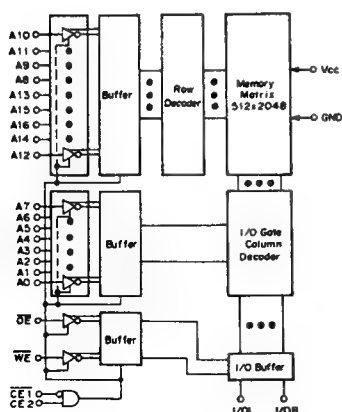
Function

131072-word × 8-bit static RAM

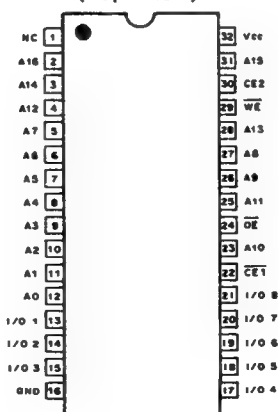
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O 0 to I/O 7	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK581000P 1.0	W
		CXK581000M 0.7	
Operating temperature	T _{opr}	- 25 to + 85	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = - 25 to + 85°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.4	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.6	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = -25 to +85°C)

Item	Symbol	Test conditions		-10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}		-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{I/O} = GND to V _{CC}		-1	—	1	-1	—	1	μA
Operating power supply current	I _{CC1}	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, V _{IN} = V _{IH} or V _{IL} I _{OUT} = 0mA		—	7	15	—	7	15	mA
Average operating current	I _{CC2}	Cycle = Min. Duty = 100%, I _{OUT} = 0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty = 100%, I _{OUT} = 0mA $\overline{CE1} \leq 0.2V$, $CE2 \geq V_{CC} - 0.2V$ $V_{IL} \leq 0.2V$, $V_{IH} \geq V_{CC} - 0.2V$	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I _{SB1}	$CE2 \leq 0.2V$ or $\overline{CE1} \geq V_{CC} - 0.2V$ $CE2 \geq V_{CC} - 0.2V$	-25 to 85°C	—	—	200	—	—	40	μA
			-25 to 70°C	—	—	100	—	—	20	
			-25 to 40°C	—	—	20	—	—	4	
			+25°C	—	2	8	—	0.7	2	
	I _{SB2}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$	—	0.6	3	—	0.6	3	3	mA
Output high voltage	V _{OH}	I _{OH} = -1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

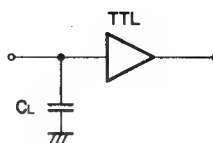
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics**● AC test conditions** $(V_{CC} = 5V \pm 10\%, T_a = -25 \text{ to } +85^\circ\text{C})$

Item	Conditions
Input pulse high level	$V_{IH} = 2.4V$
Input pulse low level	$V_{IL} = 0.6V$
Input rise time	$t_r = 5ns$
Input fall time	$t_f = 5ns$
Input and output reference level	1.5V
Output load conditions	$C_L^* = 100pF, 1TTL$

* C_L includes scope and jig capacitances



• Read cycle ($\overline{WE} = "H"$)

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	100	—	120	—	150	—	ns
Address access time	t _{AA}	—	100	—	120	—	150	ns
Chip enable access time (CE1)	t _{CO1}	—	100	—	120	—	150	ns
Chip enable access time (CE2)	t _{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t _{OE}	—	50	—	60	—	70	ns
Output hold from address change	t _{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	—	35	—	40	—	50	ns
Chip disable to output in high Z (\overline{OE})	t _{OHZ} *	—	35	—	40	—	50	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

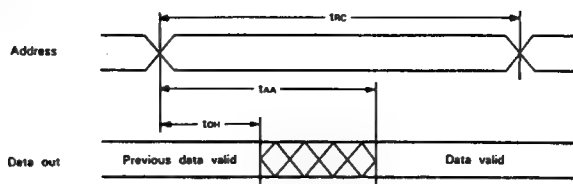
• Write cycle

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t _{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t _{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t _{DW}	40	—	50	—	60	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	70	—	80	—	90	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	5	—	5	—	5	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	—	30	—	30	—	30	ns

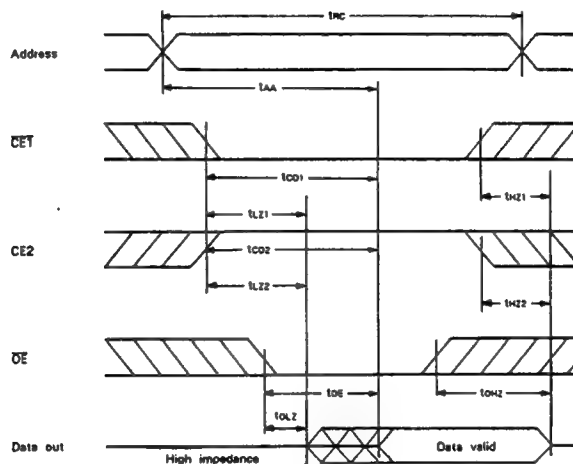
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

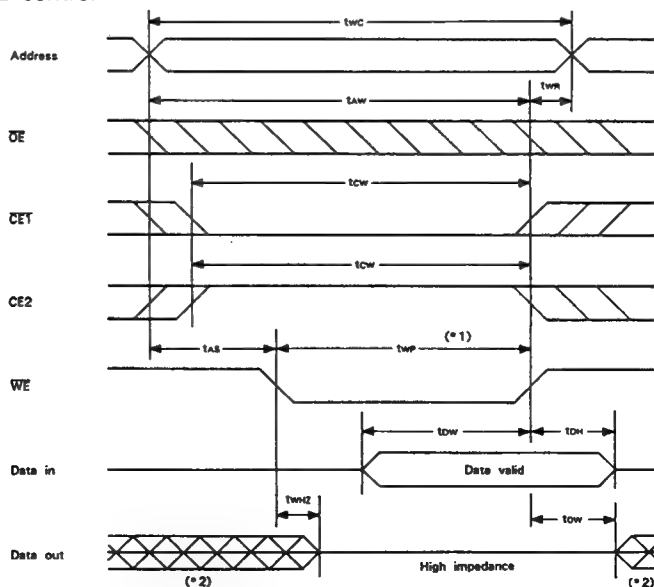
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



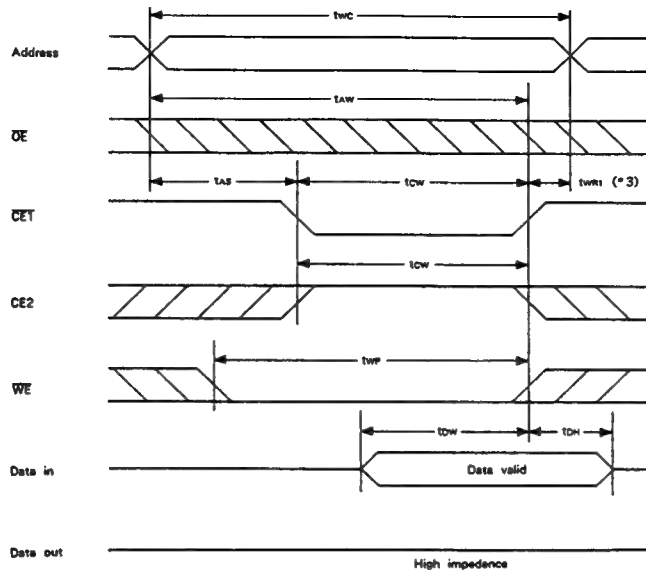
- Read cycle (2) : $\overline{WE} = V_{IH}$



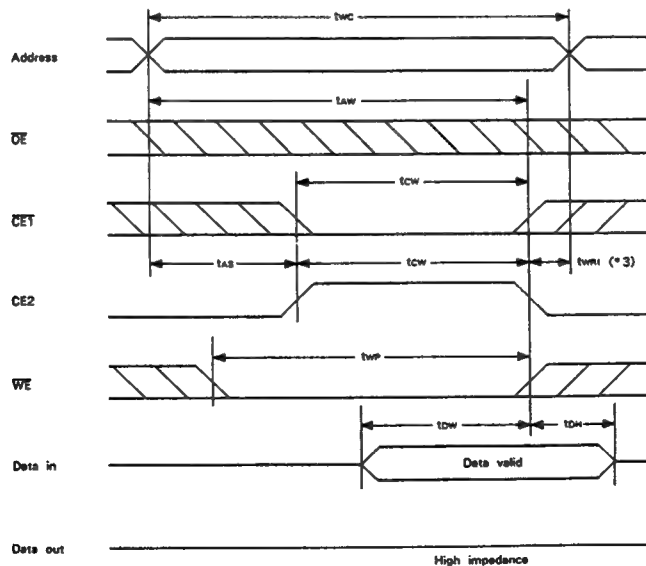
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



Note)

- *1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- *2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- *3. t_{WR1} is tested from either the rising edge of $\overline{\text{CE1}}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

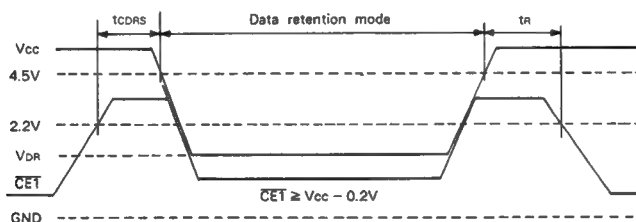
(Ta = -25 to 85°C)

Item	Symbol	Test conditions	-10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1	2.2	—	5.5	2.2	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} = 3.0V *1	-25 to 85°C	—	100	—	—	24	μA
			-25 to 70°C	—	50	—	—	12	
			-25 to 40°C	—	10	—	—	2.4	
			+25°C	—	1	—	0.4	1.2	
	I _{CCDR2}	V _{CC} = 2.2 to 5.5V *1	—	2	200	—	0.7	40	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} *2	—	—	t _{RC} *2	—	—	ns

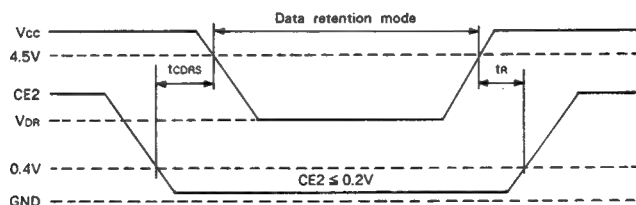
*1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)*2. t_{RC}: Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

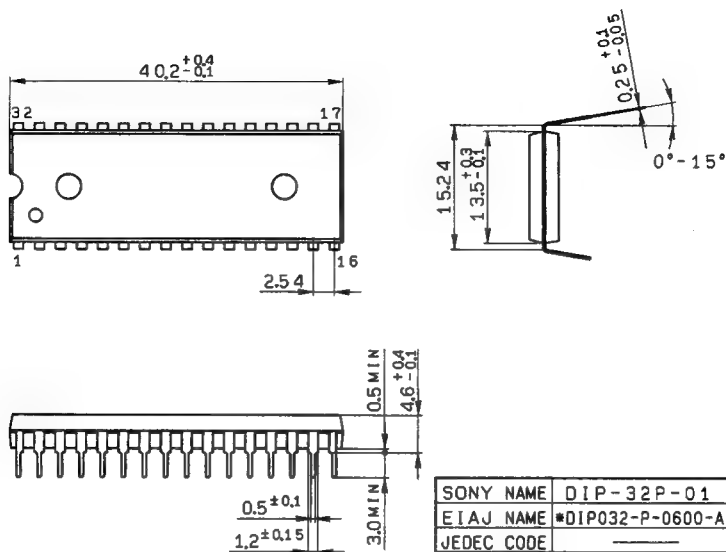


- Low supply voltage data retention waveform (2) ($CE2$ control)

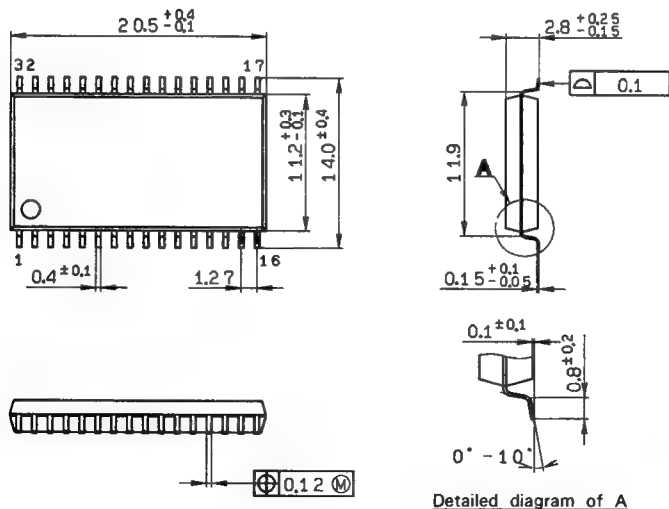


Package Outline Unit : mm

CXK581000P 32 pin DIP (Plastic) 600mil 4.5g



CXK581000M 32 pin SOP (Plastic) 525mil 1.2g



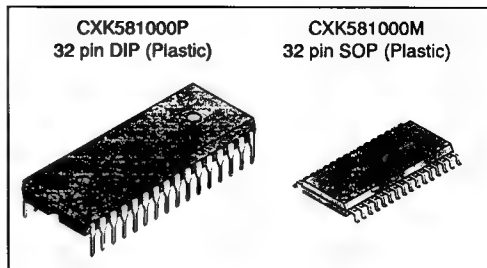
SONY NAME	SOP-32P-L02
EIAJ NAME	*SOP032-P-0525-A
JEDEC CODE	

131072-word × 8-bit High Speed CMOS Static RAM
Description

The CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131,072 words by 8 bits. Operating on a single 2.7 to 5.5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

Features

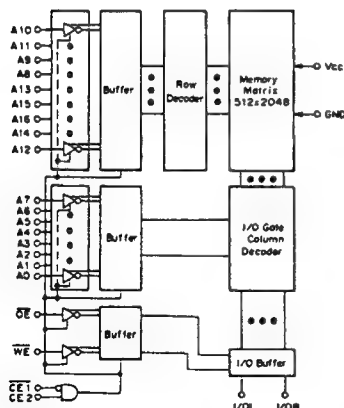
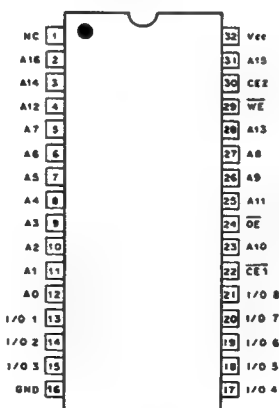
- Wide supply voltage range operation: 2.7 to 5.5V
- Fast access time: (Access time)
 - 3V Operation; 240ns (Max.)
 - 5V Operation; 120ns (Max.)
- Low power consumption operation:
 - Standby/ DC operation
 - 3V Operation; 3 μ W (Typ.) / 1.2mW (Typ.)
 - 5V Operation; 10 μ W (Typ.) / 35mW (Typ.)
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three state output.
- Directly TTL compatible: All inputs and outputs.
- Low voltage data retention: 2.0V (Min.)
- CXK581000P 600mil 32 pin DIP package
- CXK581000M 525mil 32 pin SOP package


Function

131,072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram

Pin Configuration
(Top View)

Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	2.7 to 5.5V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK581000P	1.0
		CXK581000M	0.7
Operating temperature	T _{opr}	0 to +70	℃
Storage temperature	T _{stg}	-55 to +150	℃
Soldering temperature • time	T _{solder}	260 • 10	℃ • sec

* V_{IN}, V_{IO}=-3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O pin	V _{CC} current
H	x	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
x	L	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	x	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

x : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	V _{CC} =5V ± 10%			V _{CC} =2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V _{CC}	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	-0.3 *	—	0.4	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(GND=0V, Ta=0 to +70 °C)

Item	Symbol	Test conditions		Vcc=3V ± 10%			Vcc=5V ± 10%			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} V _{IO} =GND to V _{CC}		-1	—	1	-1	—	1	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA		—	0.4	0.8	—	7	15	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	Write cycle	—	10	15	—	35	60	mA
			Read cycle	—	10	15	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty=100% I _{OUT} =0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} -0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} -0.2V	Write cycle	—	5	10	—	10	20	mA
			Read cycle	—	2.5	5	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} -0.2V or CE2 ≥ V _{CC} -0.2V	0 to +70 °C	—	—	60	—	—	100	μA
			0 to +40 °C	—	—	12	—	—	20	
			+25 °C	—	1.2	5	—	2	8	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	0.06	0.3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.2	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* Ta=25 °C

I/O Capacitance

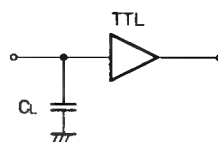
(Ta=25 °C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics**● AC test conditions**(V_{CC}=2.7 to 5.5V, T_a=0 to +70 °C)

Item	Conditions	
	V _{CC} =3V	V _{CC} =5V
Input pulse high level	V _{IH} =2.2V	V _{IH} =2.2V
Input pulse low level	V _{IL} =0.4V	V _{IL} =0.8V
Input rise time	t _r =5ns	t _r =5ns
Input fall time	t _f =5ns	t _f =5ns
Input and output reference level	1.5V	1.5V
Output load conditions	C _L * =100pF, 1TTL	C _L * =100pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle (\overline{WE} ="H")

Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	240	—	120	—	ns
Address access time	t _{AA}	—	240	—	120	ns
Chip enable access time (CE1)	t _{CO1}	—	240	—	120	ns
Chip enable access time (CE2)	t _{CO2}	—	240	—	120	ns
Output enable to output valid	t _{OE}	—	120	—	60	ns
Output hold from address change	t _{OH}	30	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t _{LZ1} , t _{LZ2}	20	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	10	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t _{HZ1} *, t _{HZ2} *	—	80	—	40	ns
Output disable to output in high Z (\overline{OE})	t _{OHZ} *	—	80	—	40	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

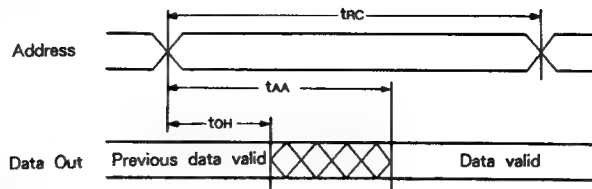
• Write cycle

Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	240	—	120	—	ns
Address valid to end of write	t _{AW}	170	—	85	—	ns
Chip enable to end of write	t _{CW}	170	—	85	—	ns
Data to write time overlap	t _{DW}	100	—	50	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	160	—	80	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t _{WR1}	0	—	0	—	ns
Output active from end of write	t _{OW}	20	—	10	—	ns
Write to output in high Z	t _{WHZ} *	—	60	—	30	ns

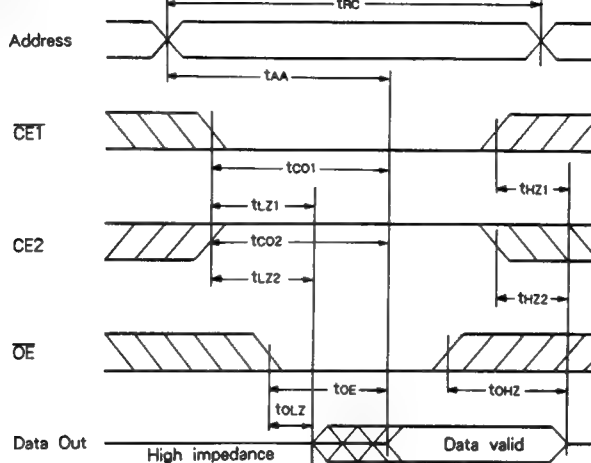
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

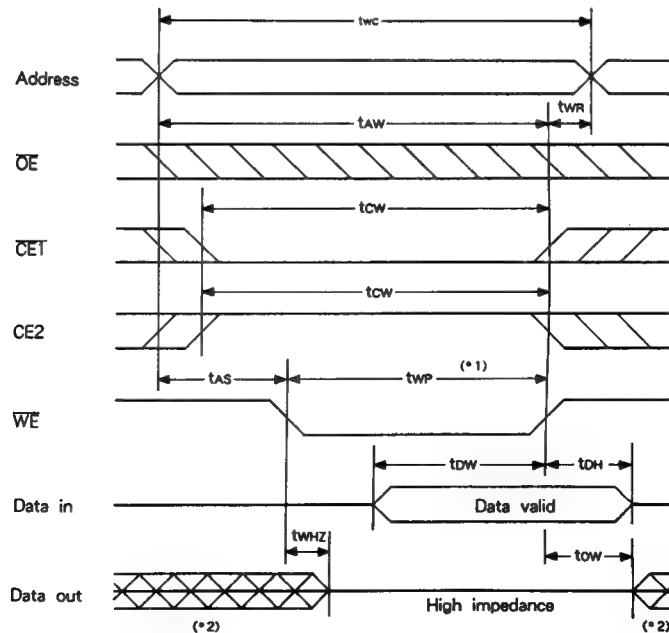
- Read cycle (1) : $\overline{CE1}=\overline{OE}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



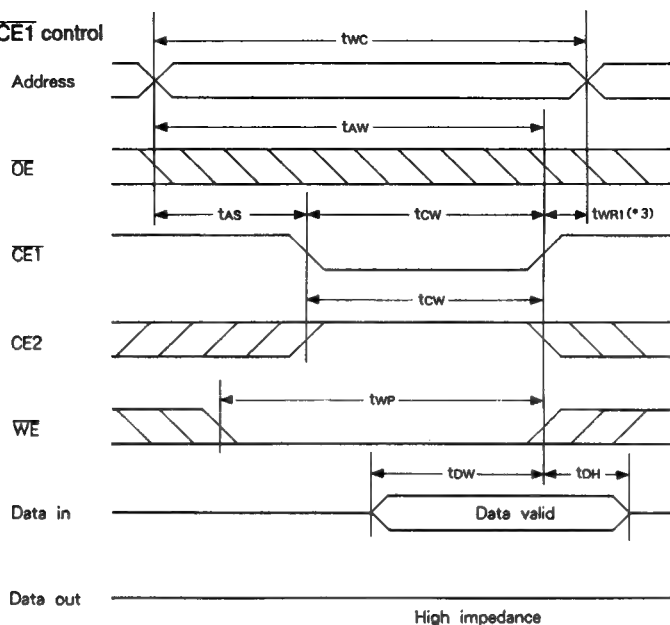
- Read cycle (2) : $\overline{WE}=V_{IH}$



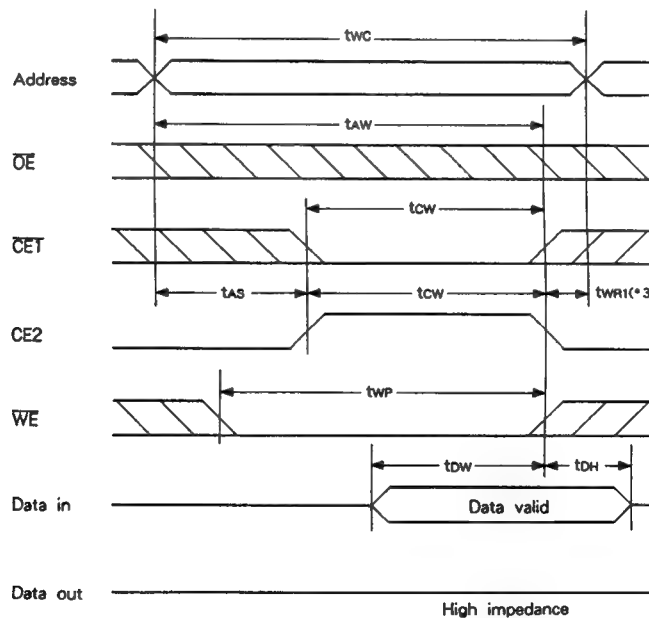
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : $\overline{CE2}$ control



- * 1. Write is executed when both $\overline{CE1}$ and \overline{WE} are at low and $\overline{CE2}$ is at high simultaneously.
- * 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- * 3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of $\overline{CE2}$, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to +70 °C)

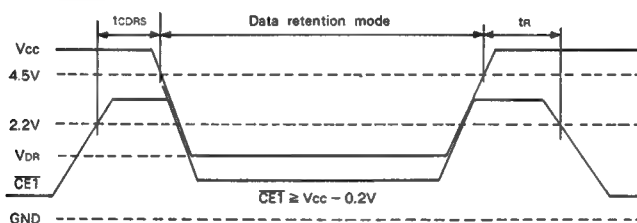
Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V _{DR}	*1		2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V *1	0 to +70 °C	—	—	50	μA
			0 to +40 °C	—	—	10	
			+25 °C	—	1	4	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V *1		—	2	100	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t _R			t _{RC} *2	—	—	ns

*1. $\overline{CE1} \geq V_{CC}-0.2V$, $CE2 \geq V_{CC}-0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

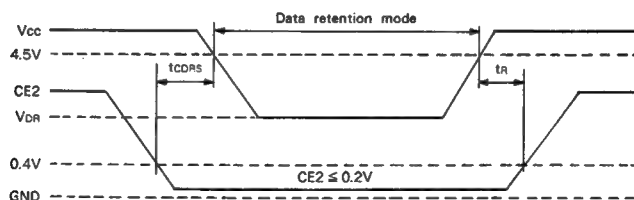
*2. t_{RC} : Read cycle time

Data Retention Waveform

- Low supply voltage data retention waveform (1) : $\overline{CE1}$ control

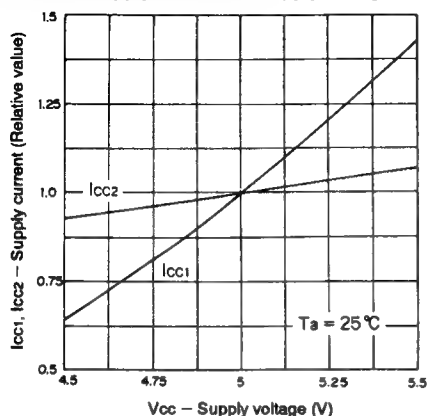


- Low supply voltage data retention waveform (2) : $CE2$ control

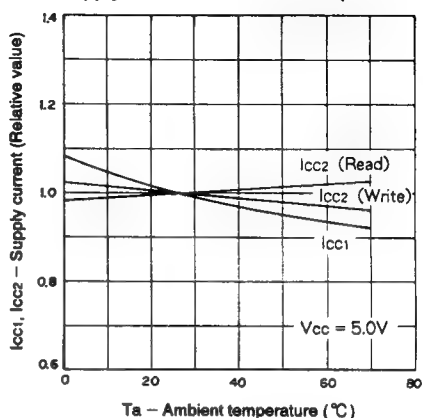


Example of Representative Characteristics

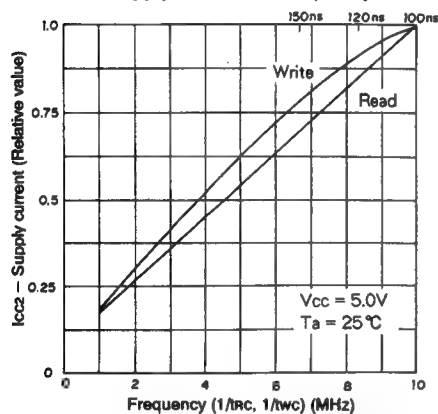
Supply current vs. Supply voltage



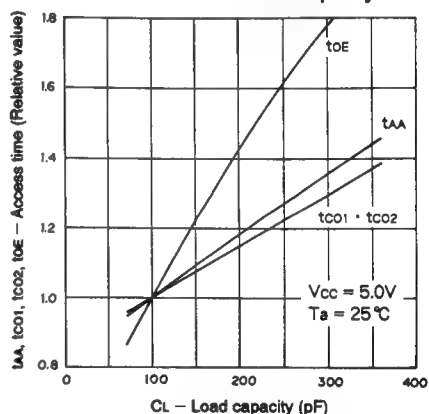
Supply current vs. Ambient temperature



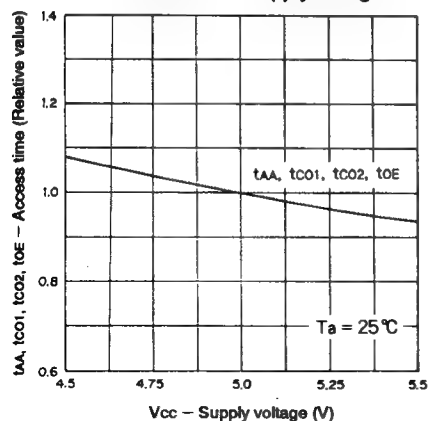
Supply current vs. Frequency



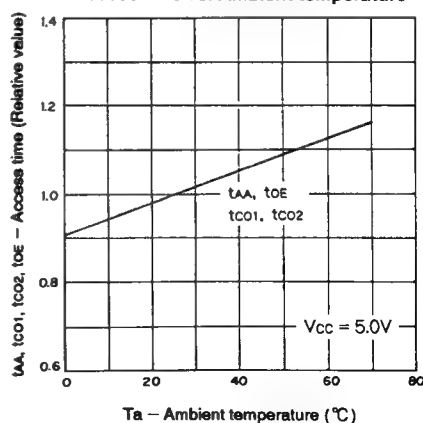
Access time vs. Load capacity



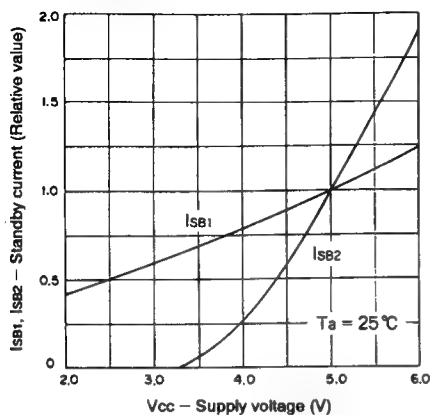
Access time vs. Supply voltage



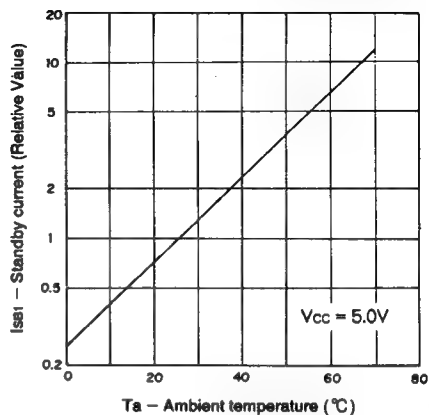
Access time vs. Ambient temperature



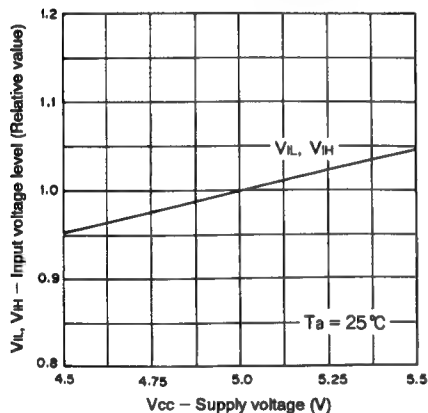
Standby current vs. Supply voltage



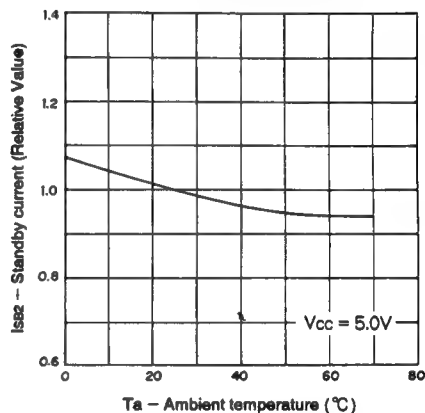
Standby current vs. Ambient temperature



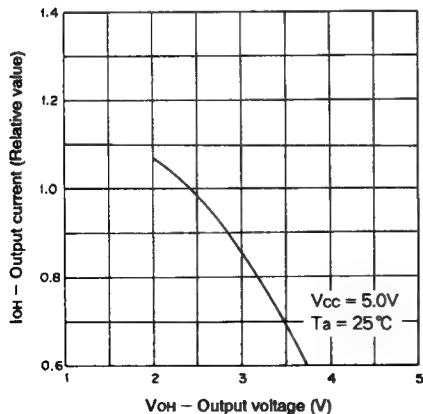
Input voltage level vs. Supply voltage



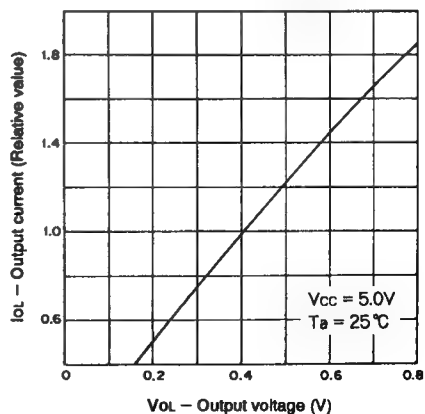
Standby current vs. Ambient temperature



Output current vs. Output voltage

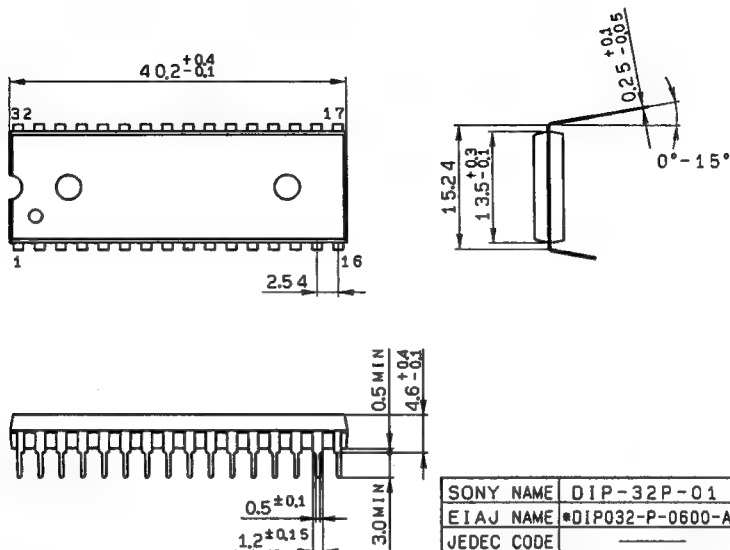


Output current vs. Output voltage

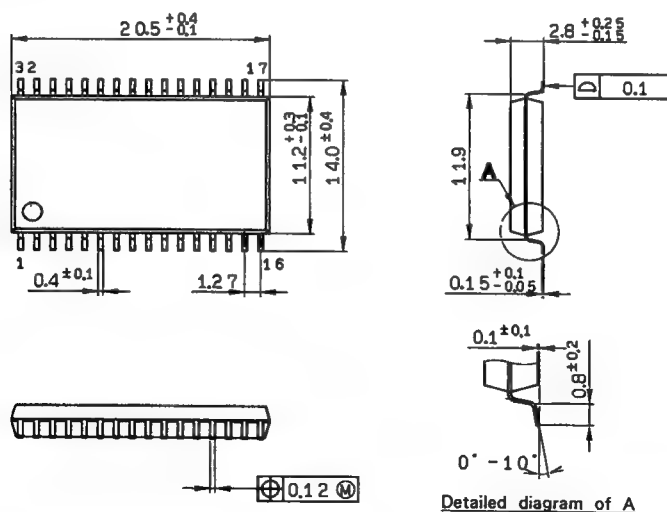


Package Outline Unit: mm

CXK581000P 32pin DIP (Plastic) 600mil 4.5g



CXK581000M 32pin SOP (Plastic) 525mil 1.2g



Detailed diagram of A

SONY NAME	SOP-32P-L02
EIAJ NAME	*SOP032-P-0525-A
JEDEC CODE	—

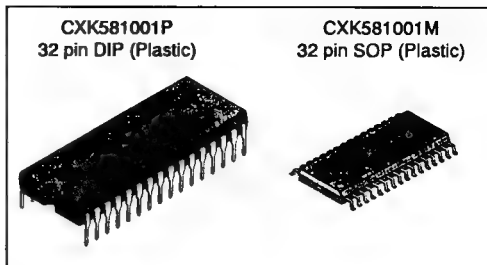
131,072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581001P/M is a 1,048,576 bits high speed CMOS static RAMs organized as 131,072 words by 8-bit and operates from a single 5V supply. This IC is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time: (Access time)
CXK581001P/M-70L/70LL 70ns (Max.)
CXK581001P/M-85L/85LL 85ns (Max.)
- Low power operation :
CXK581001P/M Standby/Operation
-70L/85L : 10 μ W (Typ.)/237.5mW (Typ., Cycle=Min.)
-70LL/85LL : 3.5 μ W (Typ.)/237.5mW (Typ., Cycle=Min.)
- Single + 5V supply : +5V \pm 10%
- Fully static memory... No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581001P 600mil 32 pin DIP package
- CXK581001M 525mil 32 pin SOP package



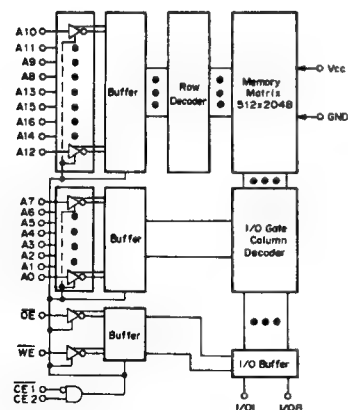
Function

131,072-word × 8-bit static RAM

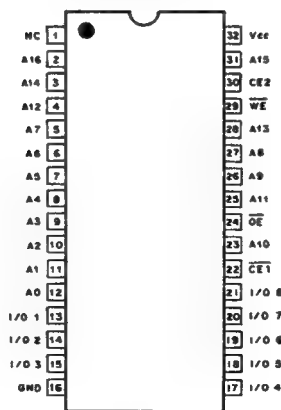
Structure

Silicon gate CMOS IC

Block diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A ₀ to A ₁₆	Address input
I/O ₁ to I/O ₈	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
V _{cc}	+5V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to +7.0	V
Input voltage	V _{IN}	- 0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{IO}	- 0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK581001P	1.0
		CXK581001M	0.7
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	- 55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{IO} = - 3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{ss1} , I _{ss2}
X	L	X	X	Not selected	High Z	I _{ss1} , I _{ss2}
L	H	H	H	Output disable	High Z	I _{cc}
L	H	L	H	Read	Data out	I _{cc}
L	H	X	L	Write	Data in	I _{cc}

X : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70 °C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	- 0.3 *	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions	- 70L/85L			- 70LL/85LL			Unit
			Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	- 1	—	1	- 1	—	1	μA
Output leakage current	I _{LO}	$\overline{CE1}=V_{IH}$ or $CE2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{I/O} =GND to V _{CC}	- 1	—	1	- 1	—	1	μA
Average operating current	I _{CC}	Cycle=Min, Duty=100% I _{OUT} =0mA	—	47.5	80	—	47.5	80	mA
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V	0 to 70 °C	—	100	—	—	20	μA
			0 to 40 °C	—	20	—	—	4	
			+25 °C	—	2	—	0.7	2	
	I _{SB2}	$\overline{CE1}=V_{IH}$ or $CE2=V_{IL}$	—	1.2	3	—	1.2	3	mA
Output high voltage	V _{OH}	I _{OH} = - 1.0mA	2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

(T_a=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

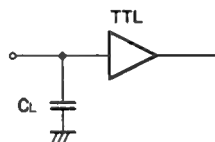
Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions

(V_{CC}=5V ± 10%, T_a=0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} =2.2V
Input pulse low level	V _{IL} =0.8V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	C _L * =100pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle (\overline{WE} ="H")

Item	Symbol	- 70L/70LL		- 85L/85LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	ns
Address access time	t _{AA}	—	70	—	85	ns
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	70	—	85	ns
Chip enable access time (CE2)	t _{CO2}	—	70	—	85	ns
Output enable to output valid	t _{OE}	—	40	—	45	ns
Output hold from address change	t _{OH}	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t _{HZ1} , t _{HZ2} *	—	25	—	25	ns
Chip disable to output in high Z (\overline{OE})	t _{OHZ} *	—	25	—	25	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

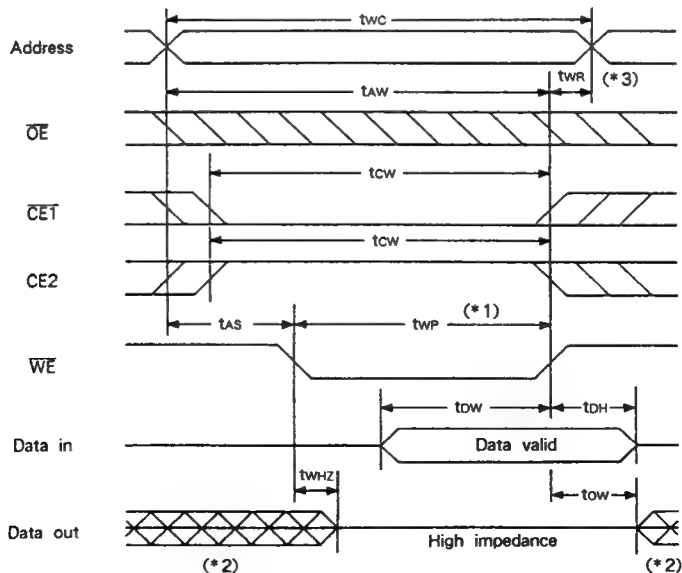
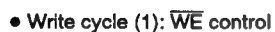
• Write cycle

Item	Symbol	- 70L/70LL		- 85L/85LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	ns
Address valid to end of write	t _{AW}	60	—	75	—	ns
Chip enable to end of write	t _{CW}	60	—	75	—	ns
Data to write time overlap	t _{DW}	25	—	30	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	60	—	ns
Address set up time	t _{AS}	0	—	0	—	ns
Write recovery time (\overline{WE} , $\overline{CE1}$)	t _{WR}	5	—	5	—	ns
Write recovery time (CE2)	t _{WR1}	10	—	10	—	ns
Output active from end of write	t _{OW}	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	—	25	—	30	ns

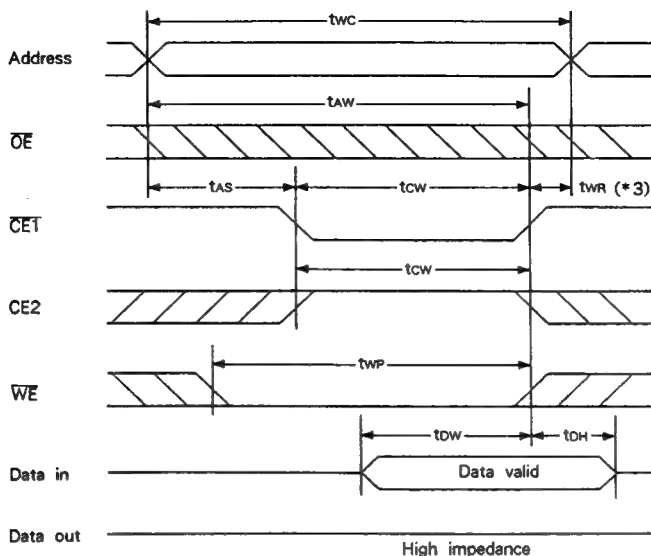
* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

- Read cycle (1): $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$

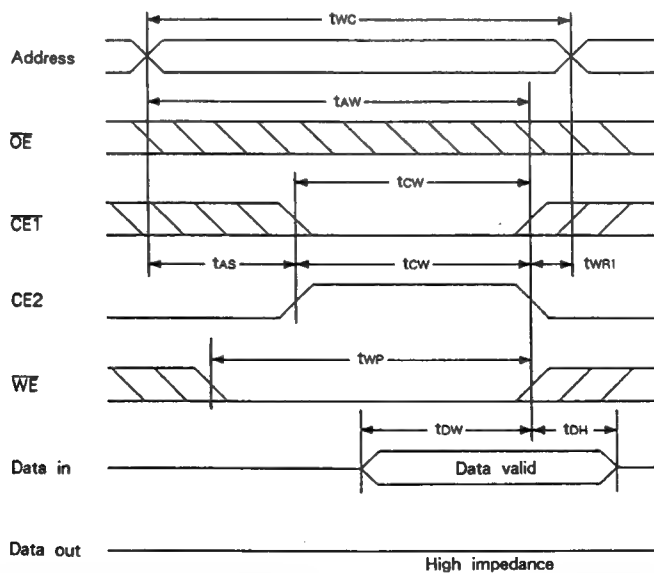
- Read cycle (1): $\overline{\text{CE1}} = \overline{\text{OE}} = V_{\text{IL}}$, $\text{CE2} = V_{\text{IH}}$, $\overline{\text{WE}} = V_{\text{IH}}$



• Write cycle (2): $\overline{\text{CE1}}$ control



• Write cycle (3): $\overline{\text{CE2}}$ control



- * 1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and $\overline{\text{CE2}}$ is at high simultaneously.
- * 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- * 3. t_{WR} is tested from the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE1}}$, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

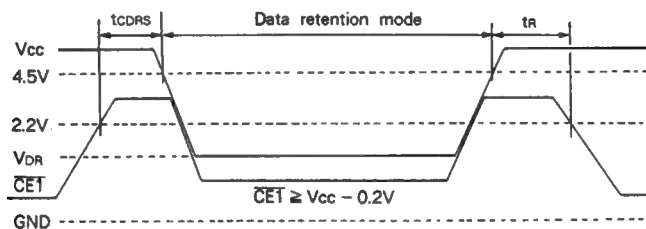
(Ta=0 to 70 °C)

Item	Symbol	Test conditions	- 70L/85L			- 70LL/85LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =0.3V *1	0 to 70 °C	—	50	—	—	12	μA
			0 to 40 °C	—	10	—	—	2.4	
			+25 °C	—	1	—	0.4	1.2	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V *1	—	2	100	—	0.7	20	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} *2	—	—	t _{RC} *2	—	—	ns

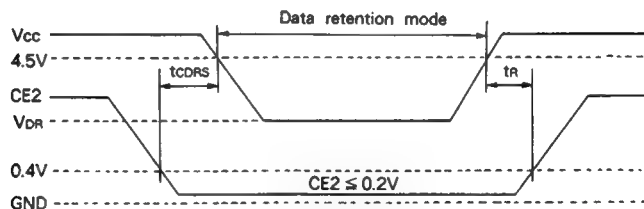
* 1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)* 2. t_{RC} : Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

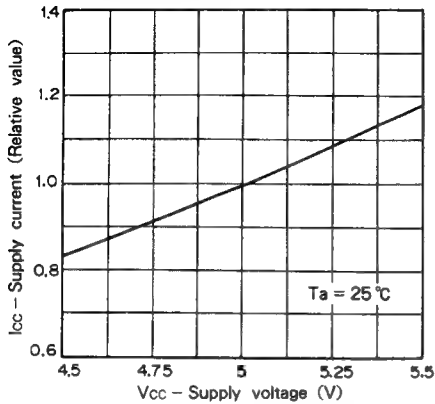


- Low supply voltage data retention waveform (2) ($CE2$ control)

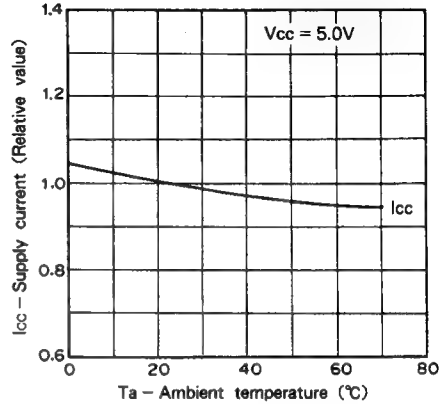


Example of Representative Characteristics

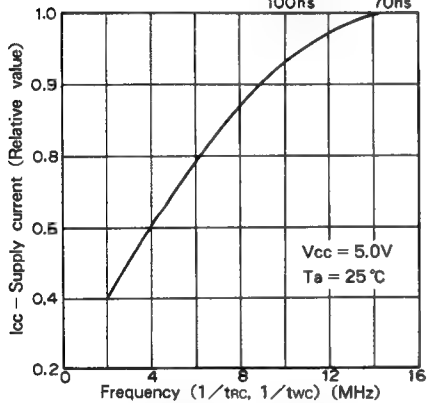
Supply current vs. Supply voltage



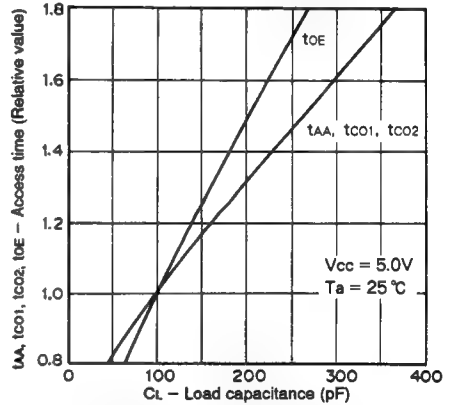
Supply current vs. Ambient temperature



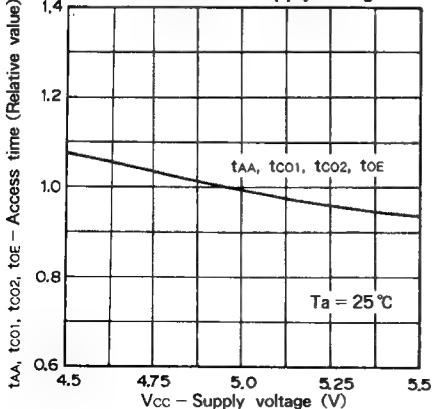
Supply current vs. Frequency



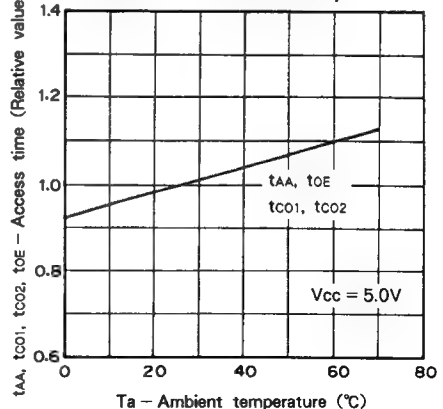
Access time vs. Load capacitance



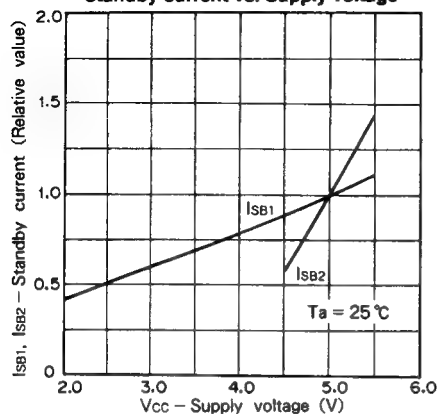
Access time vs. Supply voltage



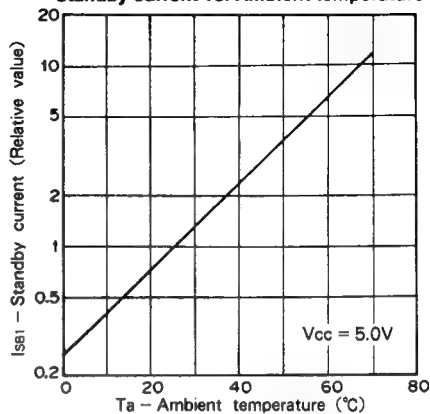
Access time vs. Ambient temperature



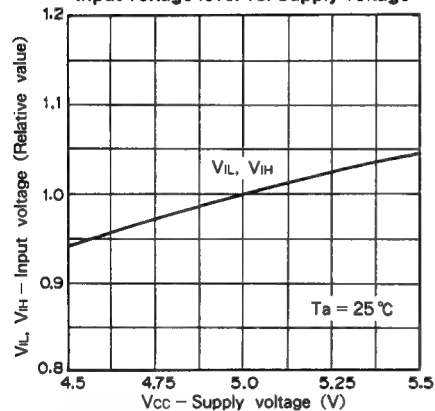
Standby current vs. Supply voltage



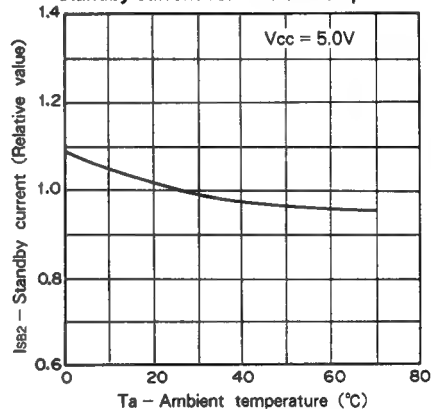
Standby current vs. Ambient temperature



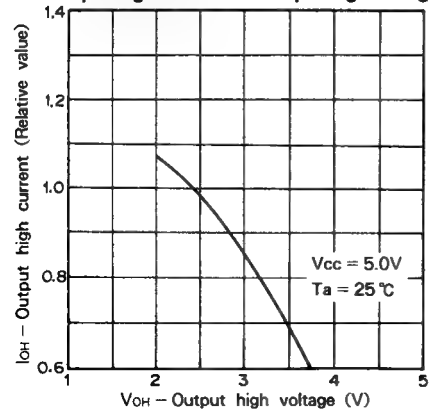
Input voltage level vs. Supply voltage



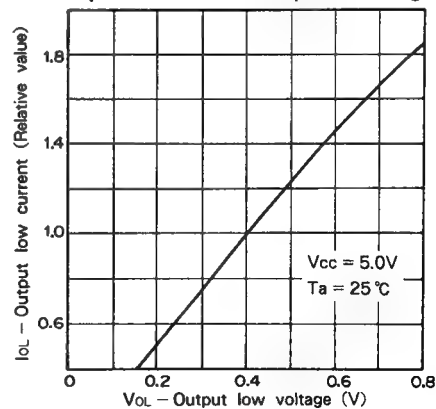
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



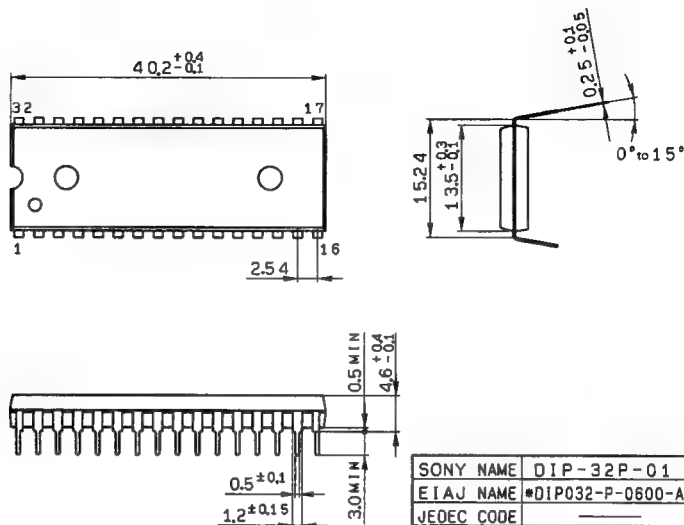
Output low current vs. Output low voltage



Package Outline Unit : mm

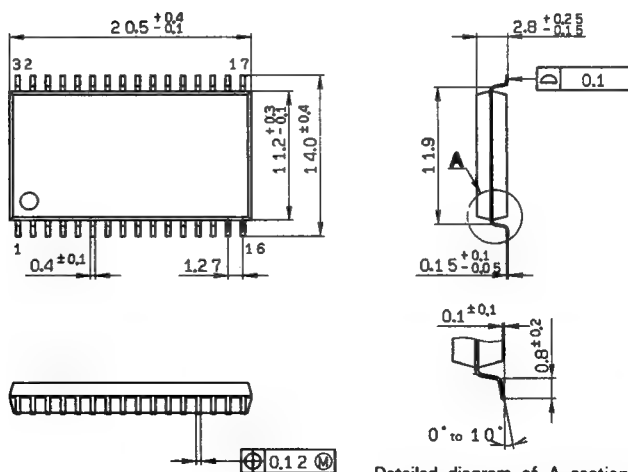
CXK581001P

32 pin DIP (Plastic) 600mil 4.5g



CXK581001M

32 pin SOP (Plastic) 525mil 1.2g



SONY. CXK581100TM/YM -10L/12L/15L
-10LL/12LL/15LL

CXK581100TM/YM

-10L/12L/15L

-10LL/12LL/15LL

131072-word \times 8-bit High Speed CMOS Static RAM

Description

CXK581100TM/YM is a 1M bits, 131072 words by 8 bits, CMOS static RAM. It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current.

Features

- Thin Small-outline Packages of EIAJ standard :
 CXK581100TM :
 8mm × 20mm 32 pin TSOP
 CXK581100YM :
 8mm × 20mm 32 pin TSOP (Mirror image pinout)
- Low stand-by current :
 L-Version :
 100 μ A (Max.) @Vcc=5.5V, Ta=0 to 70 °C
 LL-Version :
 20 μ A (Max.) @Vcc=5.5V, Ta=0 to 70 °C
- Low voltage data retention : 2.0V (Min.)
- Fast access time : (Access time)
 CXK581100TM/YM-10L, -10LL 100ns (Max.)
 CXK581100TM/YM-12L, -12LL 120ns (Max.)
 CXK581100TM/YM-15L, -15LL 150ns (Max.)
- Single +5V Supply : +5V \pm 10%

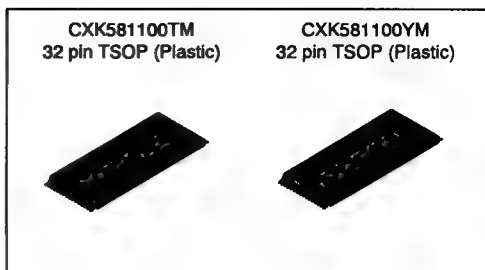
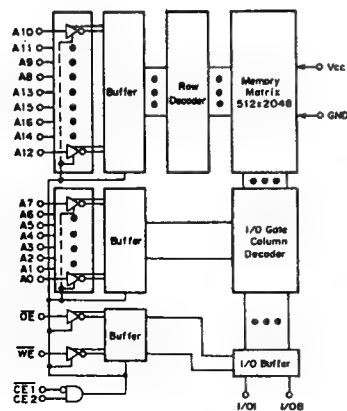
Function

131072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

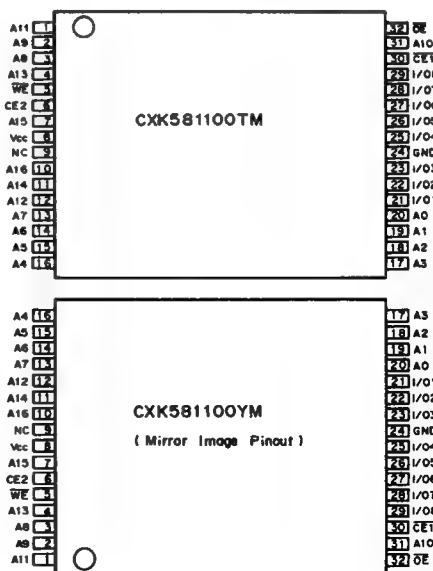
Block Diagram



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}1, CE2$	Chip enable 1, 2 input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
V _{cc}	+5V power supply
GND	Ground
NC	No connection

Pin Configuration (Top View)



E90609 - ST

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 * to +7.0	V
Input voltage	V _{IN}	- 0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{IO}	- 0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	- 55 to +150	°C
Soldering temperature * time	T _{solder}	235 * 10	°C * sec

* V_{IN}, V_{IO} = - 3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O pin	V _{CC} Current
H	x	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
x	L	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	x	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

x : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	- 0.3 *	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions		- 10L/12L/15L			- 10LL/12LL/15LL			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		- 1	—	1	- 1	—	1	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} V _{I/O} =GND to V _{CC}		- 1	—	1	- 1	—	1	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA		—	7	15	—	7	15	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty=100% I _{OUT} =0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} - 0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} - 0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V CE1 ≥ V _{CC} - 0.2V or CE2 ≥ V _{CC} - 0.2V	0 to 70 °C	—	—	100	—	—	20	μA
			0 to 40 °C	—	—	20	—	—	4	
			+25 °C	—	2	8	—	0.7	2	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	0.6	3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} = - 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

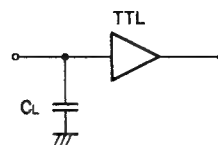
(T_a=25 °C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics**• AC test conditions** ($V_{CC}=5V \pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$)

Item	Conditions
Input pulse high level	$V_{IH}=2.2V$
Input pulse low level	$V_{IL}=0.8V$
Input rise time	$t_r=5ns$
Input fall time	$t_f=5ns$
Input and output reference level	1.5V
Output load conditions	$C_L^* = 100pF$, 1TTL

• Test circuit

* C_L includes scope and jig capacitances.

• Read cycle (\overline{WE} ="H")

Item	Symbol	– 10L/10LL		– 12L/12LL		– 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE2}$)	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	15	—	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, $\overline{CE2}$)	t_{LZ1} , t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, $\overline{CE2}$)	t_{HZ1} *, t_{HZ2} *	—	35	—	40	—	50	ns
Output disable to output in high Z (\overline{OE})	t_{OHZ} *	—	35	—	40	—	50	ns

* t_{HZ1} , t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

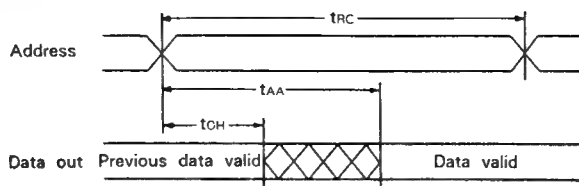
• Write cycle

Item	Symbol	– 10L/10LL		– 12L/12LL		– 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	80	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, $\overline{CE2}$)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ} *	—	30	—	30	—	30	ns

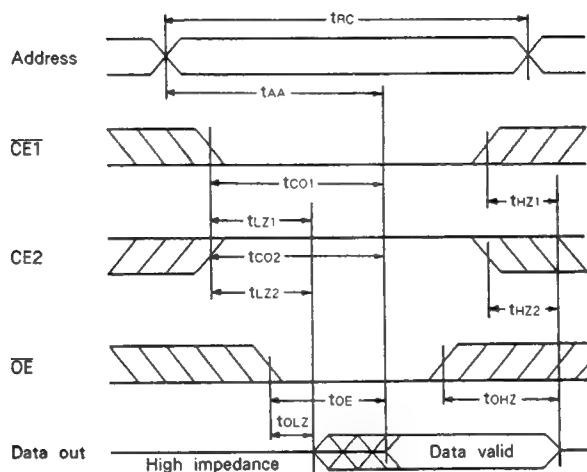
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

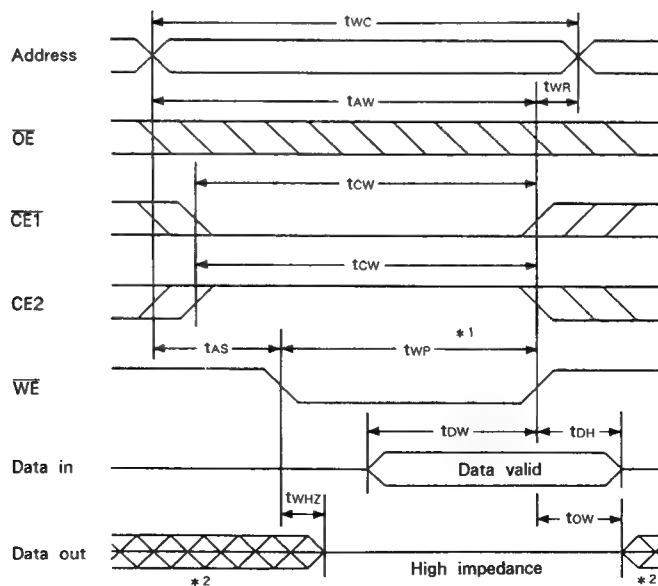
- Read cycle (1) : $\overline{CE1}=\overline{OE}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



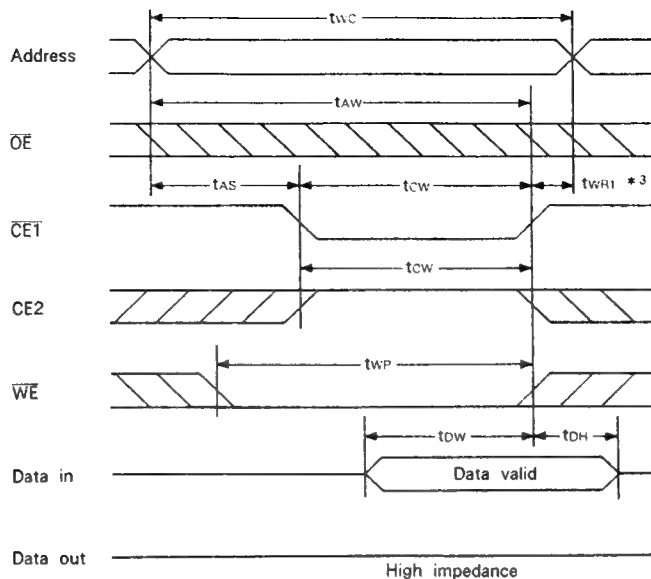
- Read cycle (2) : $\overline{WE}=V_{IH}$



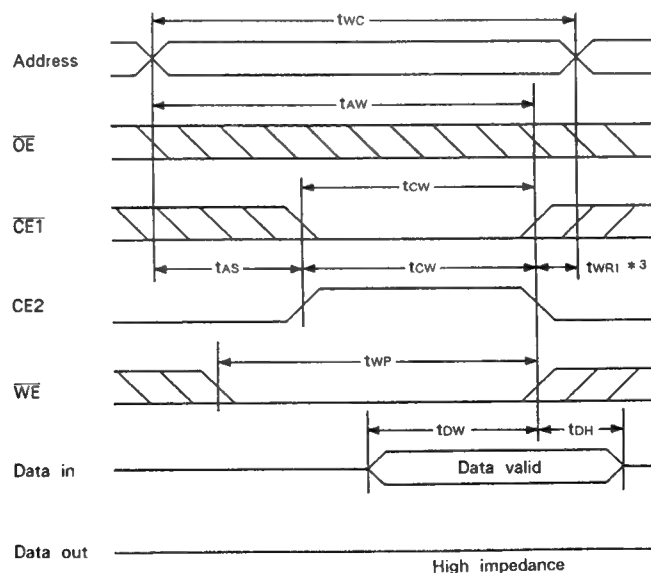
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : $\overline{CE2}$ control



Note)

- * 1. Write is executed when both $\overline{CE1}$ and \overline{WE} are at low and $\overline{CE2}$ is at high simultaneously.
- * 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- * 3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of $\overline{CE2}$, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to 70 °C)

Item	Symbol	Test conditions	- 10L/12L/15L			- 10LL/12LL/15LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	* 1	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V * 1	0 to 70 °C	—	50	—	—	12	μA
			0 to 40 °C	—	10	—	—	2.4	
			+25 °C	—	1	—	0.4	1.2	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V * 1	—	2	100	—	0.7	20	mA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _r		t _{RC} * 2	—	—	t _{RC} * 2	—	—	ns

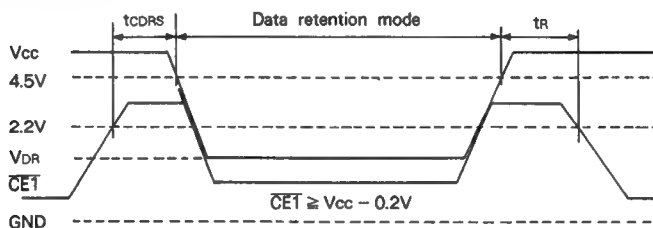
Note

* 1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

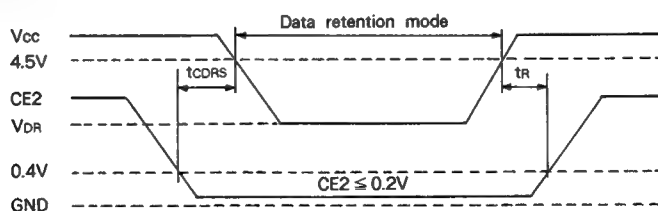
* 2. t_{RC} : Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

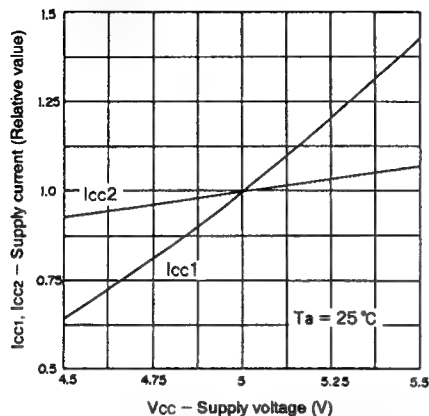


- Low supply voltage data retention waveform (2) ($CE2$ control)

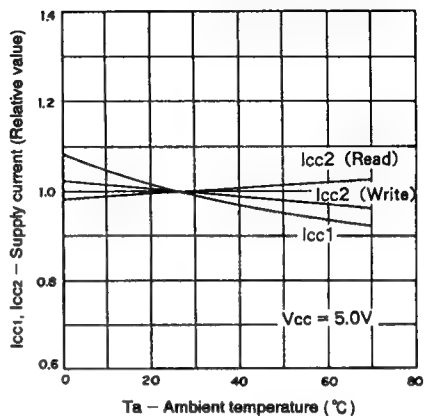


Example of Representative Characteristics

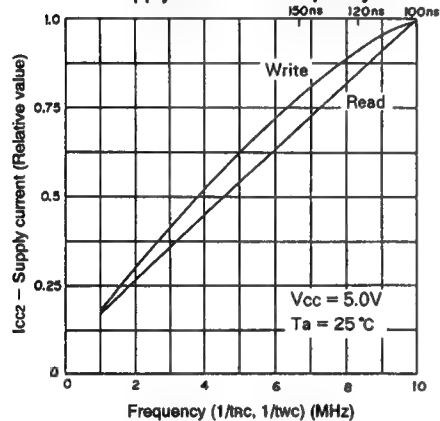
Supply current vs. Supply voltage



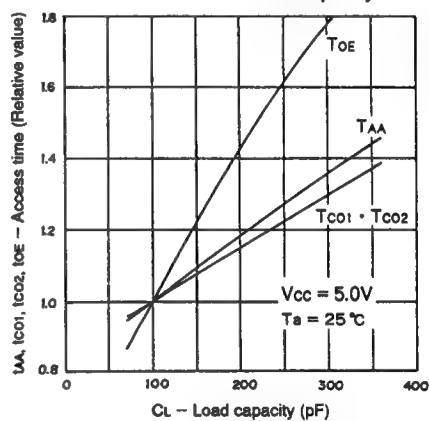
Supply current vs. Ambient temperature



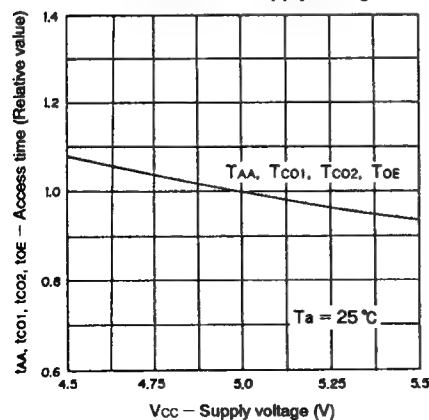
Supply current vs. Frequency



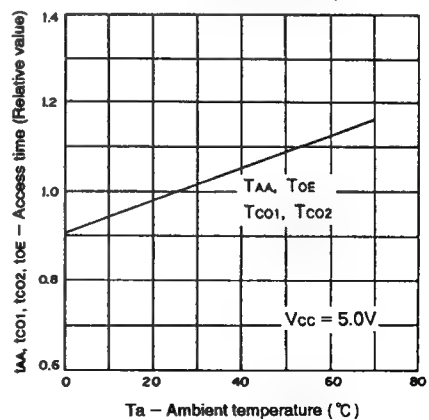
Access time vs. Load capacity



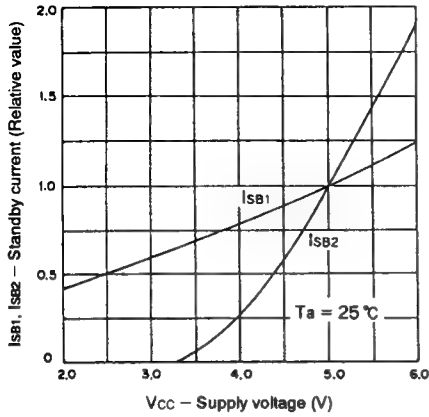
Access time vs. Supply voltage



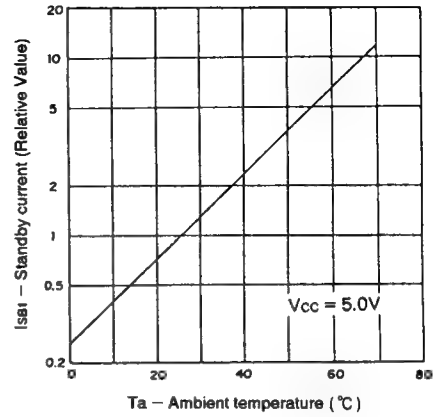
Access time vs. Ambient temperature



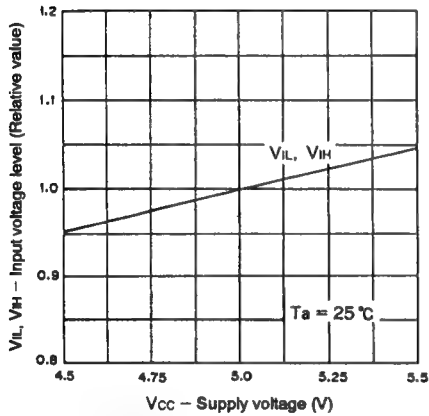
Standby current vs. Supply voltage



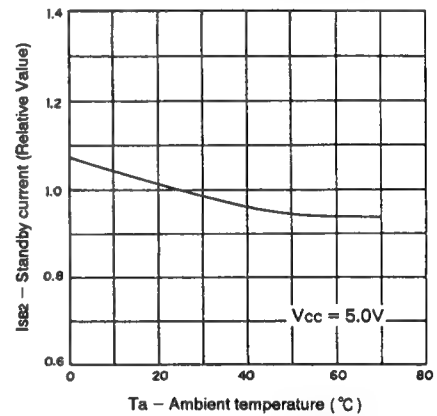
Standby current vs. Ambient temperature



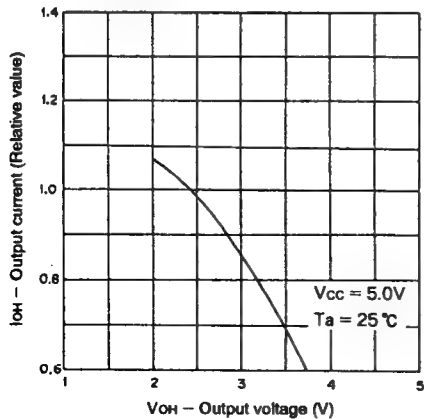
Input voltage level vs. Supply voltage



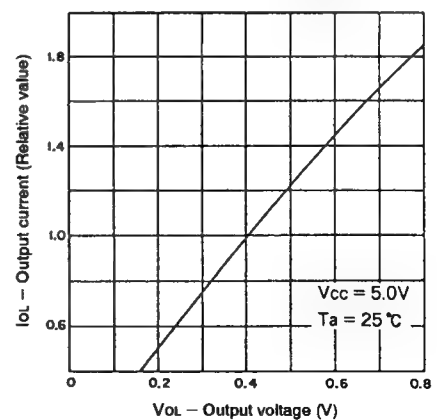
Standby current vs. Ambient temperature



Output current vs. Output voltage

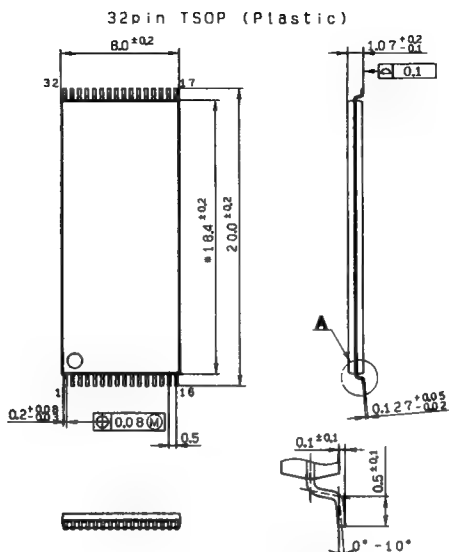


Output current vs. Output voltage



Package Outline Unit: mm

CXK581100TM

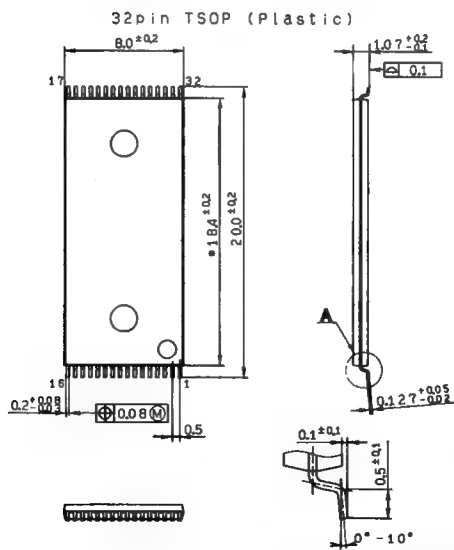


Note) Dimensions marked with * do not include mold radius.

Enlarged diagram of A

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	

CXK581100YM



Note) Dimensions marked with * do not include mold radius.

Enlarged diagram of A

SONY NAME	TSOP-32P-L01R
EIAJ NAME	TSOP032-P-0820-B
JEDEC CODE	

SONY. CXK581100TM/YM -10LX/12LX/15LX
-10LLX/12LLX/15LLX

131072-word \times 8-bit High Speed CMOS Static RAM

Description

CXK581100TM/YM is a 1M bits, 131,072 words by 8 bits, CMOS static RAM. It is suitable for portable and battery back-up systems by adopting TSOP packages correspond to extending operating temperature range and low power consumption.

Features

- Extended operating temperature range (-25 to +85 °C)
- Thin small-outline packages of EIAJ standard:
CXX581100TM:
8mm × 20mm 32 pin TSOP
CXX581100YM:
8mm × 20mm 32 pin TSOP (Mirror image pinout)
- Low stand-by current:
LX-Version:
200 μA (Max.) @Vcc=5.5V, Ta=-25 to +85 °C
LLX-Version:
40 μA (Max.) @Vcc=5.5V, Ta=-25 to +85 °C
- Low voltage data retention: 2.2V (Min.)
- Fast access time: (Access time)
CXX581100TM/YM-10LX, -10LLX 100ns (Max.)
CXX581100TM/YM-12LX, -12LLX 120ns (Max.)
CXX581100TM/YM-15LX, -15LLX 150ns (Max.)
- Single +5V Supply: +5V ± 10%

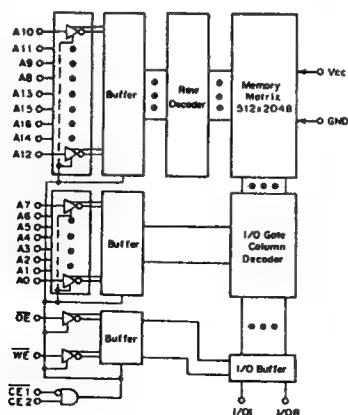
Function

131072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram



CXK581100TM
32 pin TSOP (Plastic)

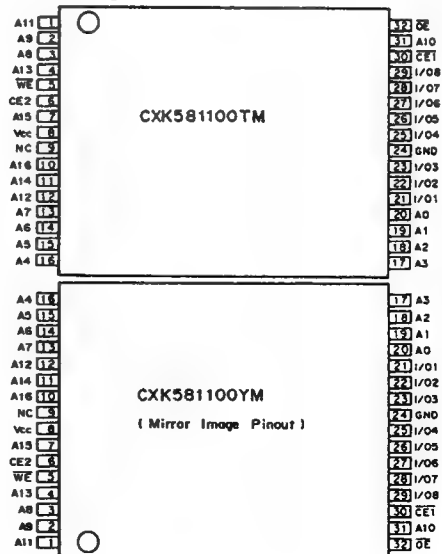
CXK581100YM
32 pin TSOP (Plastic)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}1, CE2$	Chip enable 1, 2 input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Pin Configuration (Top View)



Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	-25 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature * time	T _{solder}	235 * 10	°C * sec

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.**Truth Table**

$\overline{CE1}$	CE2	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O8	V _{CC} Current
H	x	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
x	L	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	x	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

x : "H" or "L"

DC Recommended Operating Conditions

(Ta=-25 to +85°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.4	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.6	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=−25 to +85 °C)

Item	Symbol	Test conditions		−10LX/12LX/15LX			−10LLX/12LLX/15LLX			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		−1	—	1	−1	—	1	μA
Output leakage current	I _{LO}	$\overline{CE1}=V_{IH}$ or $CE2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{I/O} =GND to V _{CC}		−1	—	1	−1	—	1	μA
Operating power supply current	I _{CC1}	$\overline{CE1}=V_{IL}$, $CE2=V_{IH}$, V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA		—	7	15	—	7	15	mA
Average operating current	I _{CC2}	Cycle=Min. Duty=100%, I _{OUT} =0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty=100%, I _{OUT} =0mA $\overline{CE1} \leq 0.2V$, $CE2 \geq V_{CC}-0.2V$ $V_{IL} \leq 0.2V$, $V_{IH} \geq V_{CC}-0.2V$	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I _{SB1}	$CE2 \leq 0.2V$ or $\overline{CE1} \geq V_{CC}-0.2V$ $CE2 \geq V_{CC}-0.2V$	−25 to +85 °C	—	—	200	—	—	40	μA
			−25 to +70 °C	—	—	100	—	—	20	
			−25 to +40 °C	—	—	20	—	—	4	
			+25 °C	—	2	8	—	0.7	2	
	I _{SB2}	$\overline{CE1}=V_{IH}$ or $CE2=V_{IL}$		—	0.6	3	—	0.6	3	mA
Output high voltage	V _{OH}	I _{OH} =−1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O Capacitance

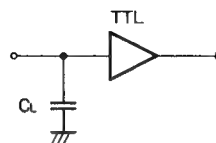
(T_a=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics**● AC test conditions** $(V_{CC}=5V \pm 10\%, T_a=-25 \text{ to } +85^\circ\text{C})$

Item	Conditions
Input pulse high level	$V_{IH}=2.4V$
Input pulse low level	$V_{IL}=0.6V$
Input rise time	$t_r=5ns$
Input fall time	$t_f=5ns$
Input and output reference level	1.5V
Output load conditions	$C_L^* = 100pF, 1TTL$



* C_L includes scope and jig capacitances

• Read cycle ($\overline{WE} = "H"$)

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	100	—	120	—	150	—	ns
Address access time	t _{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE2}$)	t _{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t _{OE}	—	50	—	60	—	70	ns
Output hold from address change	t _{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, $\overline{CE2}$)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, $\overline{CE2}$)	t _{HZ1} *, t _{HZ2} *	—	35	—	40	—	50	ns
Chip disable to output in high Z (\overline{OE})	t _{OHZ} *	—	35	—	40	—	50	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

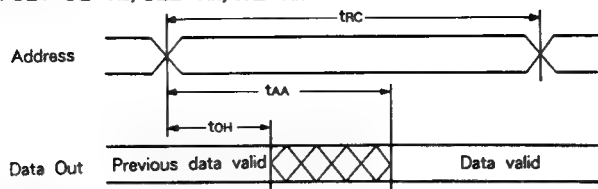
• Write cycle

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t _{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t _{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t _{DW}	40	—	50	—	60	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	70	—	80	—	90	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	5	—	5	—	5	—	ns
Write recovery time ($\overline{CE1}$, $\overline{CE2}$)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	—	30	—	30	—	30	ns

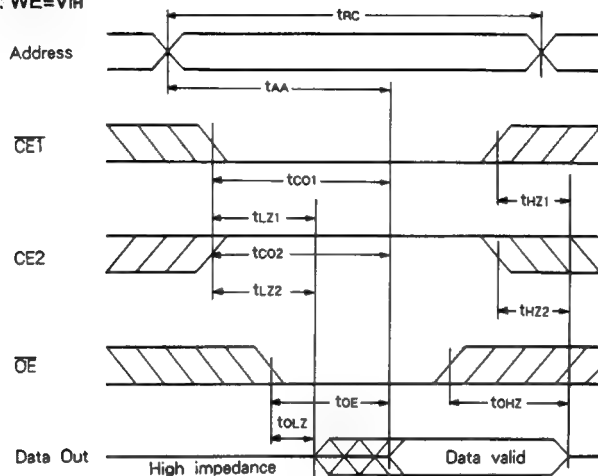
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

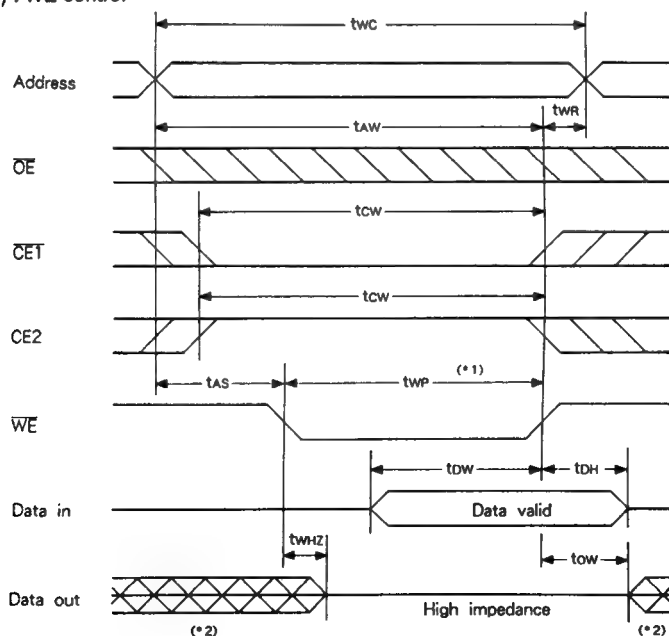
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



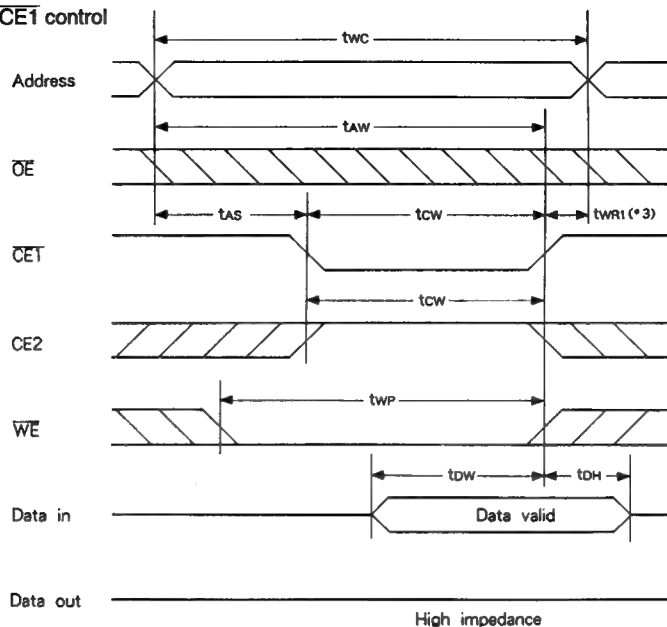
- Read cycle (2) : $\overline{WE}=V_{IH}$



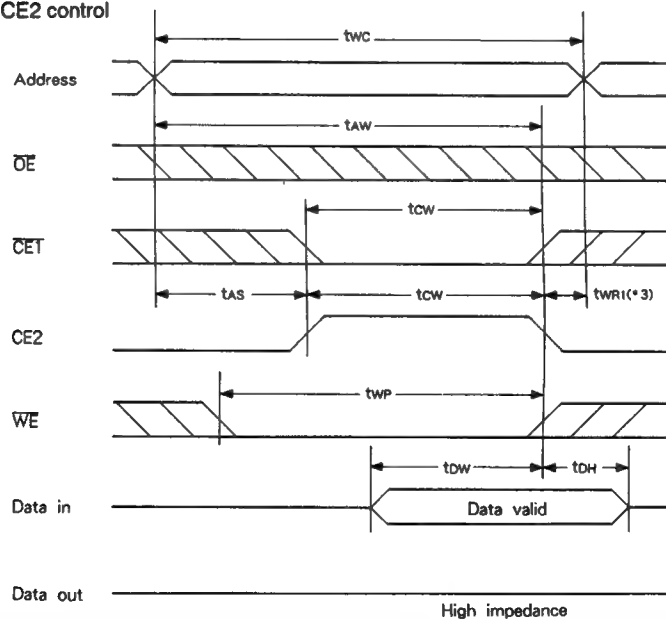
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



- * 1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- * 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- * 3. t_{wr1} is tested from either the rising edge of $\overline{\text{CE1}}$ or the falling edge of $\overline{\text{CE2}}$, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

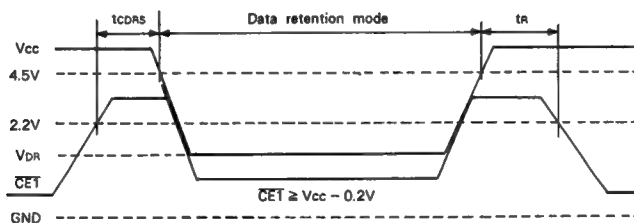
(Ta = -25 to +85 °C)

Item	Symbol	Test conditions		-10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1		2.2	—	5.5	2.2	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V *1	-25 to +85 °C	—	—	100	—	—	24	μA
			-25 to +70 °C	—	—	50	—	—	12	
			-25 to +40 °C	—	—	10	—	—	2.4	
			+25 °C	—	1	4	—	0.4	1.2	
	I _{CCDR2}	V _{CC} =2.2 to 5.5V *1		—	2 *3	200	—	0.7 *3	40	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t _R			t _{RC} *2	—	—	t _{RC} *2	—	—	ns

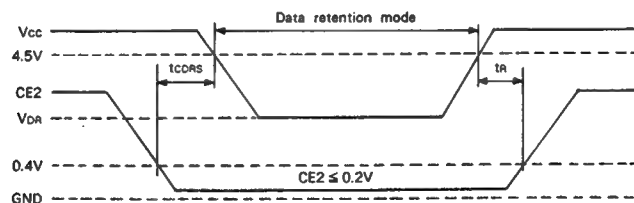
*1. $\overline{CE1} \geq V_{CC}-0.2V$, $CE2 \geq V_{CC}-0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)*2. t_{RC}: Read cycle time*3. V_{CC}=5V, Ta=25 °C

Data Retention Waveform

- Low supply voltage data retention waveform (1) : $\overline{CE1}$ control



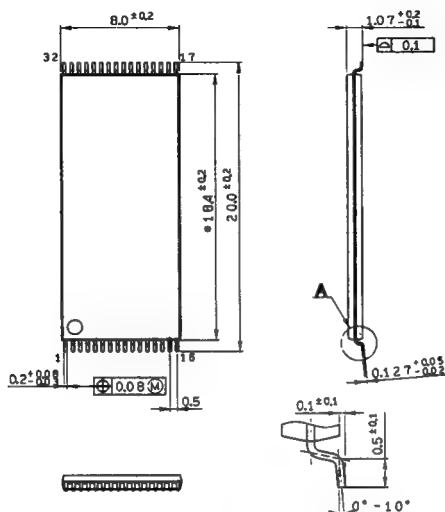
- Low supply voltage data retention waveform (2) : $CE2$ control



Package Outline Unit : mm

CXK581100TM

32pin TSOP (Plastic)



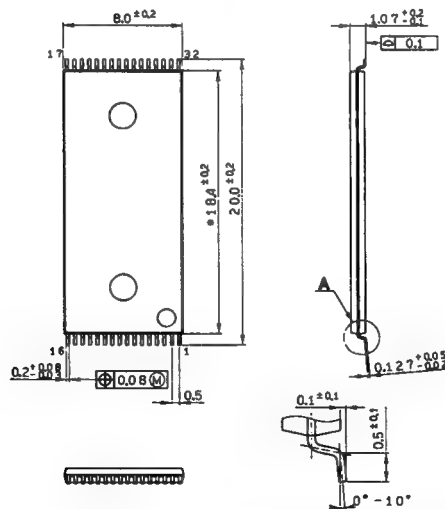
Detailed diagram of A(20/1)

Note) Dimensions marked with *
does not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP32-P-0820-A
JEDEC CODE	

CXK581100YM

32pin TSOP (Plastic)



Detailed diagram of A(20/1)

Note) Dimensions marked with *
does not include resin residue.

SONY NAME	TSOP-32P-L01R
EIAJ NAME	TSOP32-P-0820-B
JEDEC CODE	

SONY**CXK581100TM/YM** -12LB**131072-word × 8-bit High Speed CMOS Static RAM****Description**

CXK581100TM/YM is a general purpose high speed CMOS static RAM organized as 131,072 words by 8 bits. It is suitable for portable and battery back-up systems by adopting TSOP packages correspond to 2.7 to 5.5V power supply operation and low power consumption.

Features

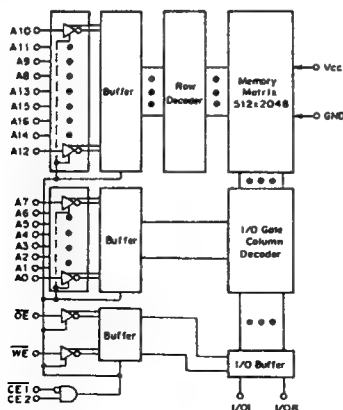
- Wide supply voltage range operation: 2.7 to 5.5V
- Thin small-outline packages of EIAJ standard:
CXK581100TM:
8mm × 20mm 32 pin TSOP
- CXK581100YM:
8mm × 20mm 32 pin TSOP (Mirror image pinout)
- Low power consumption operation:
Standby / DC operation
3V operation; 3 μ W (Typ.) / 1.2mW (Typ.)
5V operation; 10 μ W (Typ.) / 35mW (Typ.)
- Fast access time: (Access time)
3V operation; 240ns (Max.)
5V operation; 120ns (Max.)
- Low voltage data retention: 2.0V (Min.)

Function

131072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram

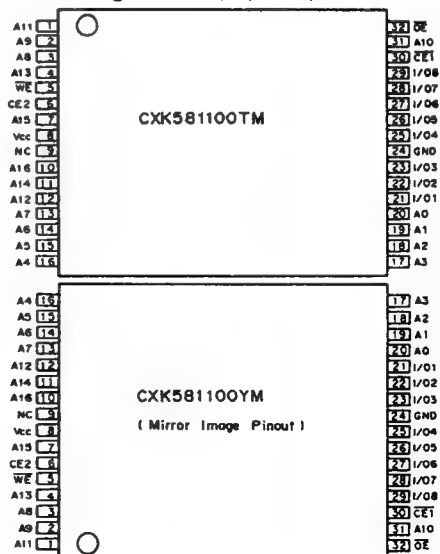
CXK581100TM
32 pin TSOP (Plastic)



CXK581100YM
32 pin TSOP (Plastic)

**Pin Description**

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	2.7 to 5.5V power supply
GND	Ground
NC	No connection

Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 * to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{IO}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	235 • 10	°C • sec

* V_{IN}, V_{IO}=-3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O pin	V _{CC} Current
H	x	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
x	L	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	x	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

x : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	V _{CC} =5V ± 10%			V _{CC} =2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V _{CC}	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	-0.3 *	—	0.4	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(GND=0V, Ta=0 to +70 °C)

Item	Symbol	Test conditions		Vcc=3V ± 10%			Vcc=5V ± 10%			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} V _{I/O} =GND to V _{CC}		-1	—	1	-1	—	1	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA		—	0.4	0.8	—	7	15	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	Write cycle	—	10	15	—	35	60	mA
			Read cycle	—	10	15	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty=100% I _{OUT} =0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} -0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} -0.2V	Write cycle	—	5	10	—	10	20	mA
			Read cycle	—	2.5	5	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} -0.2V or CE2 ≥ V _{CC} -0.2V	0 to +70 °C	—	—	60	—	—	100	μA
			0 to +40 °C	—	—	12	—	—	20	
			+25 °C	—	1.2	5	—	2	8	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	0.06	0.3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.2	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* Ta=25 °C

I/O Capacitance

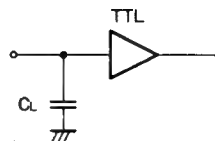
(Ta=25 °C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics**● AC test conditions**(V_{CC}=2.7 to 5.5V, T_a=0 to +70°C)

Item	Conditions	
	V _{CC} =3V	V _{CC} =5V
Input pulse high level	V _{IH} =2.2V	V _{IH} =2.2V
Input pulse low level	V _{IL} =0.4V	V _{IL} =0.8V
Input rise time	t _r =5ns	t _r =5ns
Input fall time	t _f =5ns	t _f =5ns
Input and output reference level	1.5V	1.5V
Output load conditions	C _L * =100pF, 1TTL	C _L * =100pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle (\overline{WE} ="H")

Item	Symbol	Vcc=3V \pm 10%		Vcc=5V \pm 10%		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	240	—	120	—	ns
Address access time	t _{AA}	—	240	—	120	ns
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	240	—	120	ns
Chip enable access time (CE2)	t _{CO2}	—	240	—	120	ns
Output enable to output valid	t _{OE}	—	120	—	60	ns
Output hold from address change	t _{OH}	30	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t _{LZ1} , t _{LZ2}	20	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	10	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t _{HZ1} *, t _{HZ2} *	—	80	—	40	ns
Output disable to output in high Z (\overline{OE})	t _{OHZ} *	—	80	—	40	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

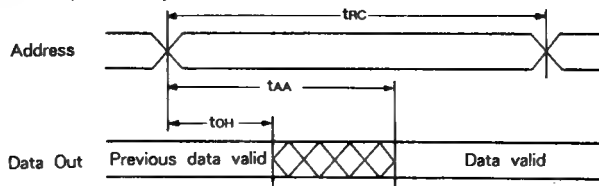
• Write cycle

Item	Symbol	Vcc=3V \pm 10%		Vcc=5V \pm 10%		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	240	—	120	—	ns
Address valid to end of write	t _{AW}	170	—	85	—	ns
Chip enable to end of write	t _{CW}	170	—	85	—	ns
Data to write time overlap	t _{DW}	100	—	50	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	160	—	80	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t _{WR1}	0	—	0	—	ns
Output active from end of write	t _{OW}	20	—	10	—	ns
Write to output in high Z	t _{WHZ} *	—	60	—	30	ns

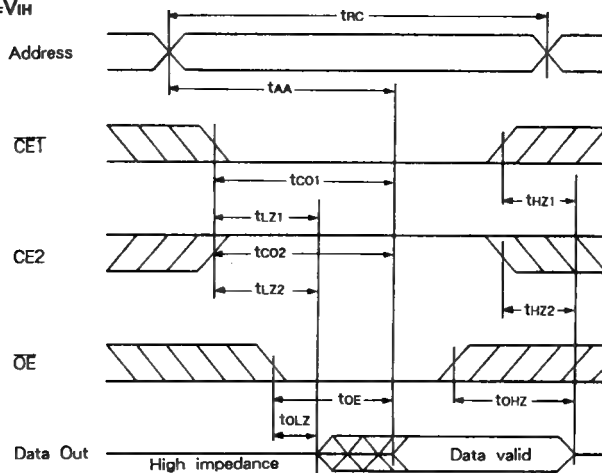
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

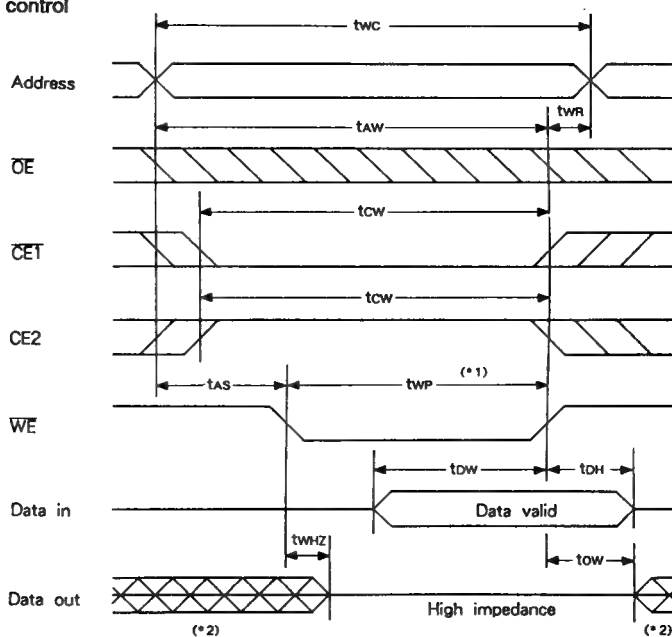
- Read cycle (1) : $\overline{CE1}=\overline{OE}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



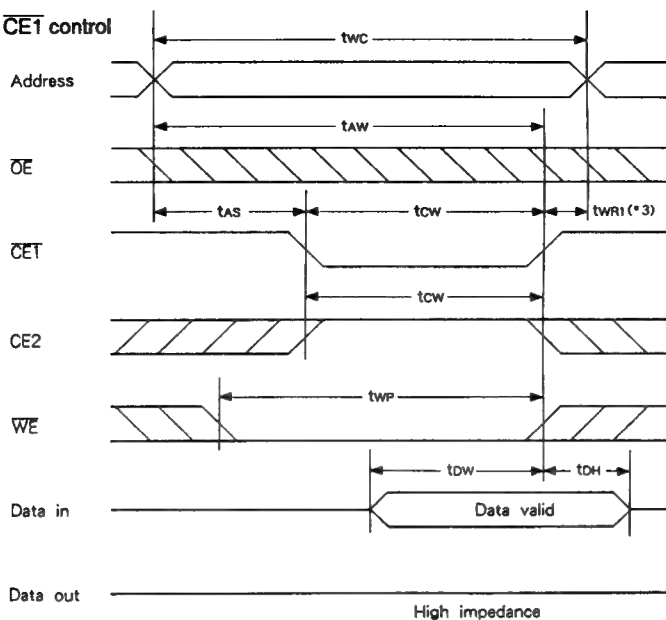
- Read cycle (2) : $\overline{WE}=V_{IH}$



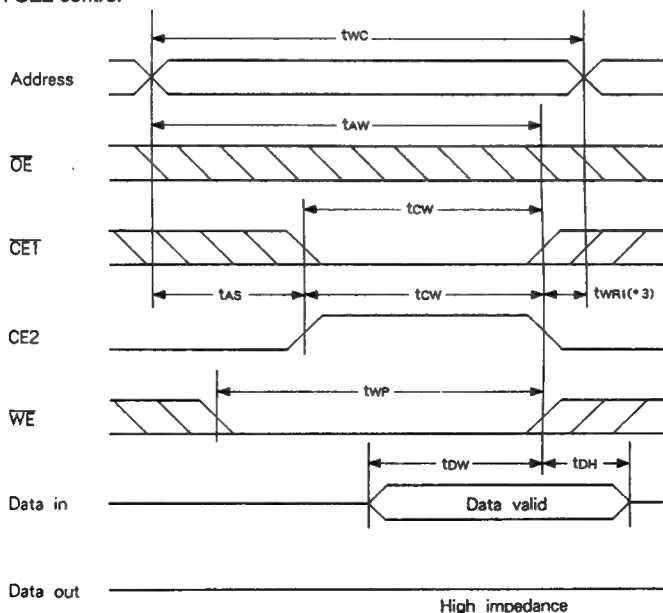
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : $\overline{\text{CE2}}$ control



* 1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and $\overline{\text{CE2}}$ is at high simultaneously.

* 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

* 3. t_{WH1} is tested from either the rising edge of $\overline{\text{CE1}}$ or the falling edge of $\overline{\text{CE2}}$, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to +70°C)

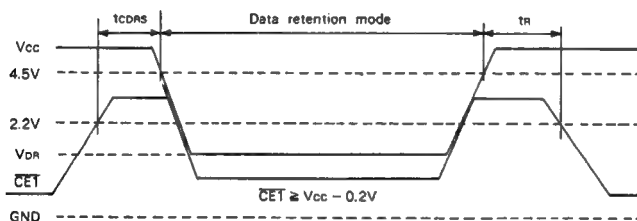
Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V _{DR}	* 1		2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V * 1	0 to +70°C	—	—	50	μA
			0 to +40°C	—	—	10	
			+25°C	—	1	4	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V * 1		—	2	100	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t _r			t _{RC} * 2	—	—	ns

* 1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

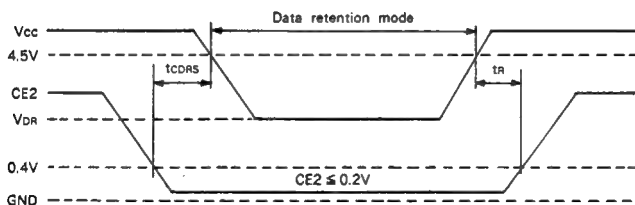
* 2. t_{RC} : Read cycle time

Data Retention Waveform

- Low supply voltage data retention waveform (1) : $\overline{CE1}$ control

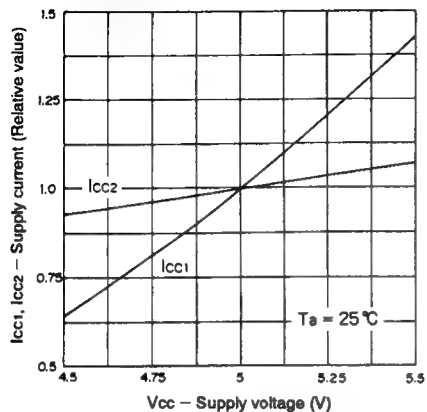


- Low supply voltage data retention waveform (2) : $CE2$ control

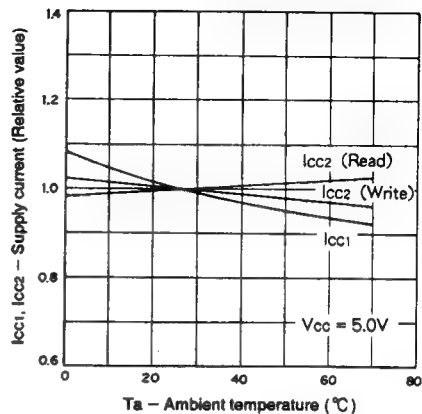


Example of Representative Characteristics

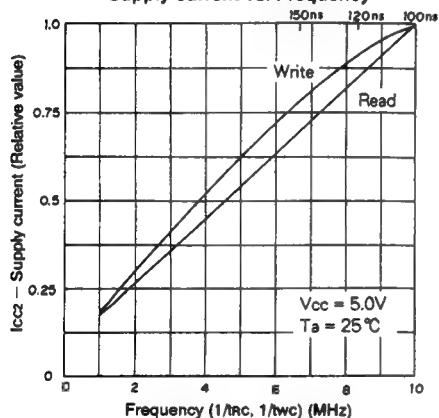
Supply current vs. Supply voltage



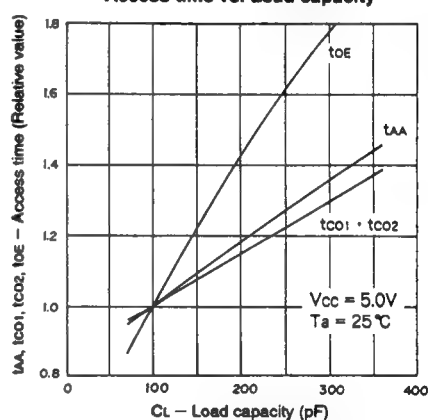
Supply current vs. Ambient temperature



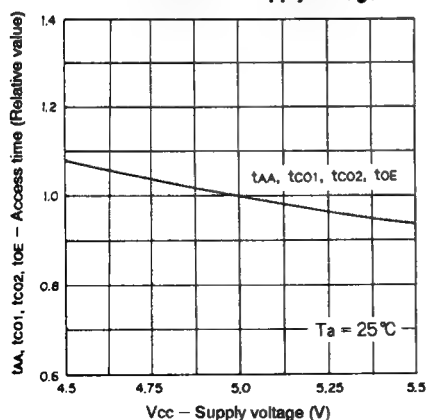
Supply current vs. Frequency



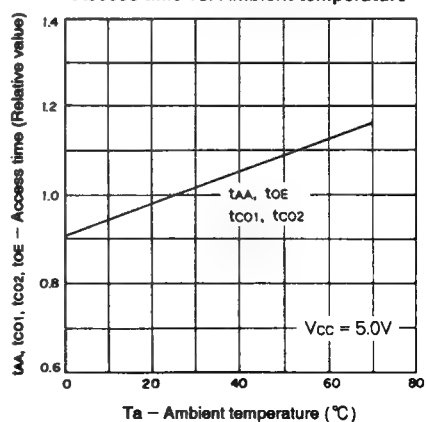
Access time vs. Load capacity



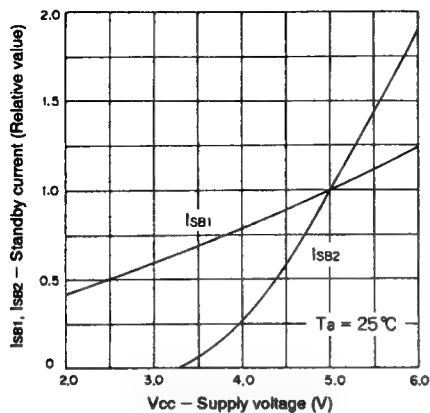
Access time vs. Supply voltage



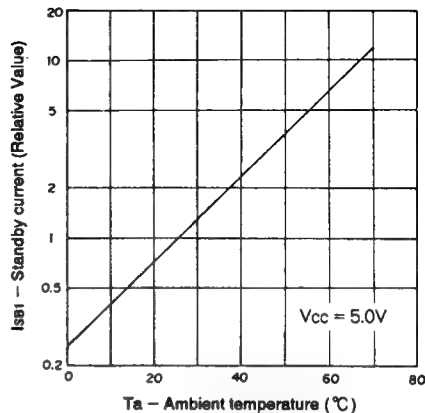
Access time vs. Ambient temperature



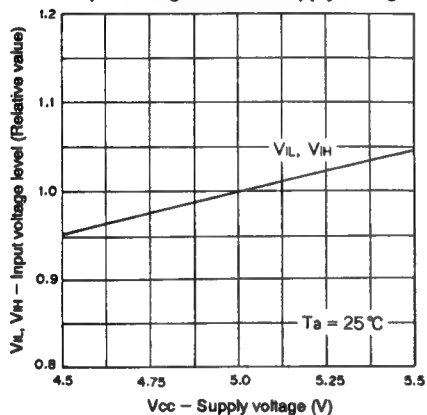
Standby current vs. Supply voltage



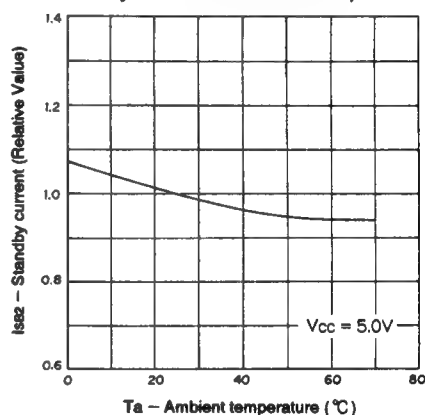
Standby current vs. Ambient temperature



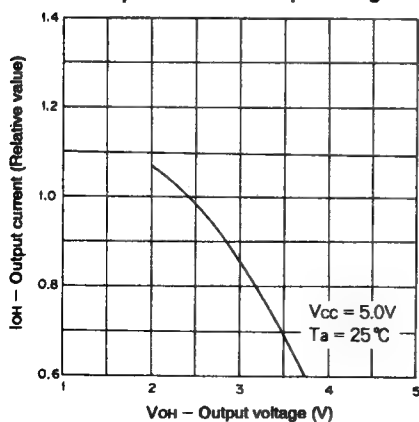
Input voltage level vs. Supply voltage



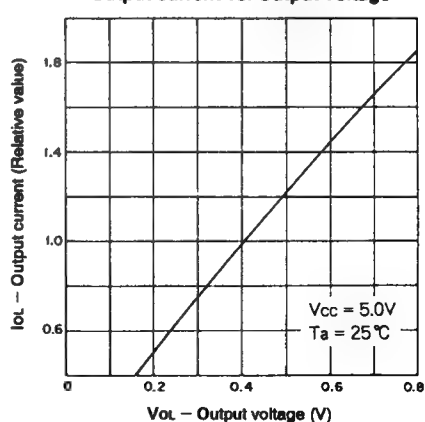
Standby current vs. Ambient temperature



Output current vs. Output voltage



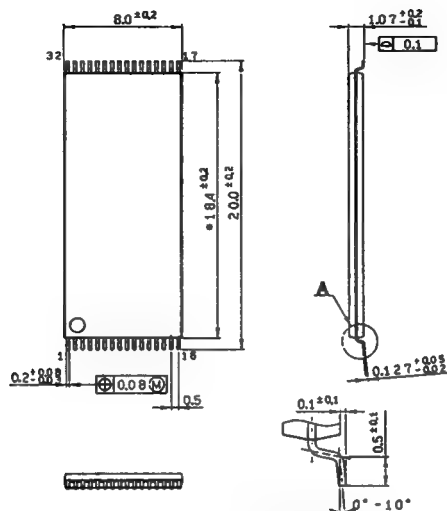
Output current vs. Output voltage



Package Outline Unit : mm

CXK581100TM

32pin TSOP (Plastic)



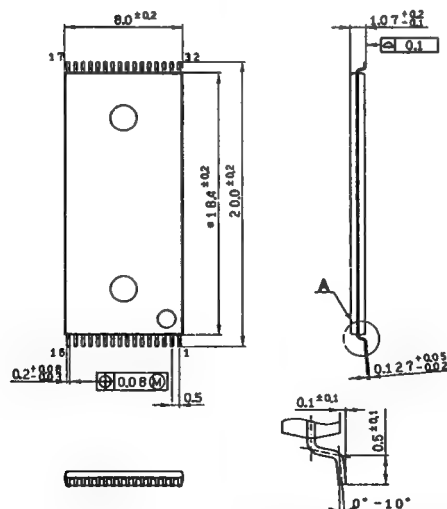
Detailed diagram of A(20/1)

Note) Dimensions marked with *
does not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	

CXK581100YM

32pin TSOP (Plastic)



Detailed diagram of A(20/1)

Note) Dimensions marked with *
does not include resin residue.

SONY NAME	TSOP-32P-L01R
EIAJ NAME	TSOP032-P-0820-B
JEDEC CODE	

SONY**CXK581020SP/J** -35/45/55**131072-word × 8-bit High Speed CMOS Static RAM****Description**

CXK581020SP/J are 131,072-word × 8-bit high speed CMOS static RAMs suitable for use in high speed and low power applications.

Organized as 131,072 words by 8 bits, it operates from a single 5V supply.

Features

- Fast access time : (Access time)
CXK581020SP/J-35 35ns (Max.)
CXK581020SP/J-45 45ns (Max.)
CXK581020SP/J-55 55ns (Max.)
- Low power operation : (Operation)
CXK581020SP/J-35, 45, 55
300mW(Typ, Cycle = Min.)
- Single +5V supply : +5V ± 10 %
- Fully static memory ... No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible : All inputs and outputs.
- Available in 32 pin 400-mil DIP and 400-mil SOJ

CXK581020SP
32 pin DIP (Plastic)

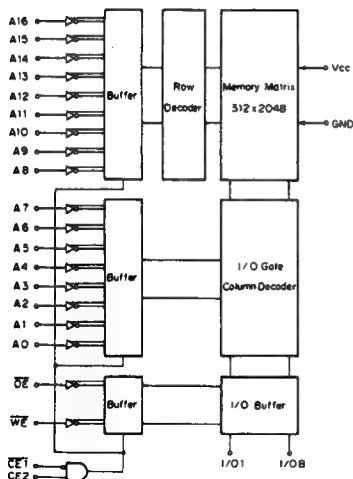
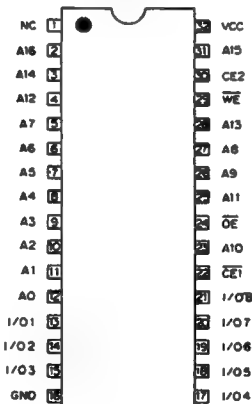
CXK581020J
32 pin SOJ (Plastic)

**Function**

131,072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration
(Top View)****Pin Description**

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* **Note)** V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} current
H	x	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
x	L	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC2}
L	H	L	H	Read	Data out	I _{CC2}
L	H	x	L	Write	Data in	I _{CC2}

Note) x : "H" or "L"**DC Recommended Operating Conditions** (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* **Note)** V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-2	—	2	μA
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , $\overline{CE1} = V_{IH}$ or CE2 = V _{IL} or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-2	—	2	μA
Operating power supply current	I _{CC1}	$\overline{CE1} = V_{IL}$, CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	—	—	mA
Average operating current	I _{CC2}	Cycle = Min., Duty = 100%, I _{OUT} = 0mA	—	—	130	mA
Standby current	I _{SB1}	$\overline{CE1} \geq V_{CC} - 0.2V$ or CE2 ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	0.01	2	mA
	I _{SB2}	$\overline{CE1} = V_{IH}$ or CE2 = V _{IL} , Cycle = Min.	—	—	55	mA
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* Note) V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

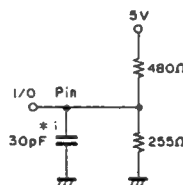
Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)*2

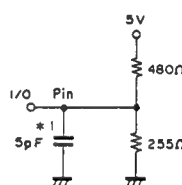
*1. C_L includes scope and jig capacitances.*2. For t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	-35		-45		-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	35	—	45	—	55	—	ns
Address access time	t _{AA}	—	35	—	45	—	55	ns
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	35	—	45	—	55	ns
Chip enable access time (CE2)	t _{CO2}	—	35	—	45	—	55	ns
Output enable to output valid	t _{OE}	—	20	—	25	—	30	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t _{LZ1} *, t _{LZ2} *	5	—	5	—	5	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t _{HZ1} *, t _{HZ2} *	0	15	0	20	0	25	ns
Chip disable to output in high Z (\overline{OE})	t _{OHZ} *	0	15	0	20	0	25	ns
Chip enable to power up time ($\overline{CE1}$, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip enable to power down time ($\overline{CE1}$, CE2)	t _{PD}	—	35	—	45	—	55	ns

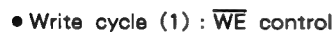
• Write cycle

Item	Symbol	-35		-45		-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t _{AW}	30	—	40	—	45	—	ns
Chip enable to end of write	t _{CW}	30	—	40	—	45	—	ns
Data to write time overlap	t _{DW}	18	—	20	—	25	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	30	—	35	—	40	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (\overline{WE} , $\overline{CE1}$)	t _{WR1}	3	—	3	—	3	—	ns
Write recovery time (CE2)	t _{WR2}	5	—	5	—	5	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	15	0	15	0	15	ns

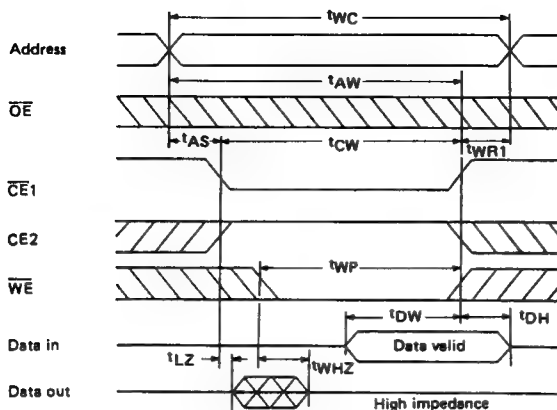
* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1 (2). This parameter is sampled and not 100% tested.

- Read cycle (1) : $\overline{\text{CE1}} = \overline{\text{OE}} = V_{\text{IL}}$, $\text{CE2} = V_{\text{IH}}$, $\overline{\text{WE}} = V_{\text{IH}}$

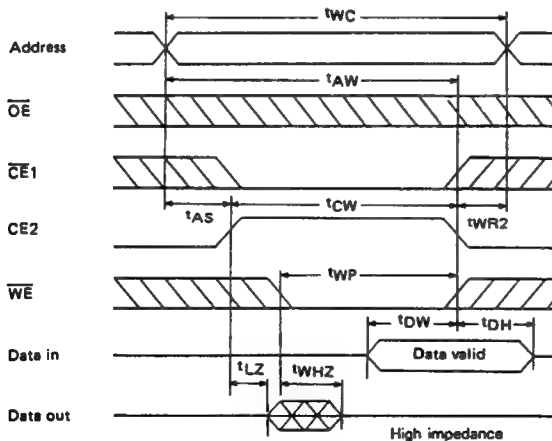
- Read cycle (1) : $\overline{\text{CE1}} = \overline{\text{OE}} = V_{\text{IL}}$, $\text{CE2} = V_{\text{IH}}$, $\overline{\text{WE}} = V_{\text{IH}}$



• Write cycle (2) : $\overline{CE1}$ control



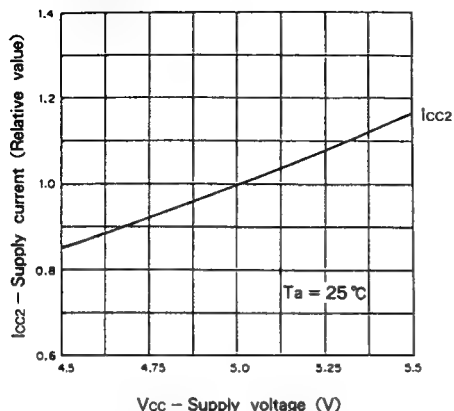
• Write cycle (3) : $\overline{CE2}$ control



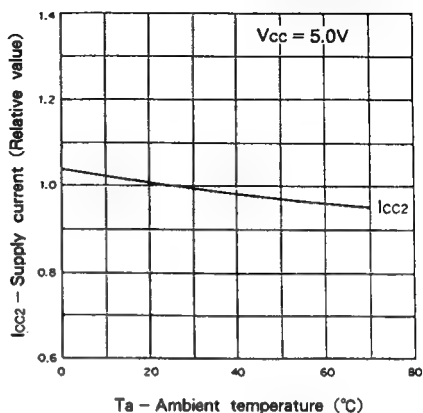
Note) During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Example of Representative Characteristics

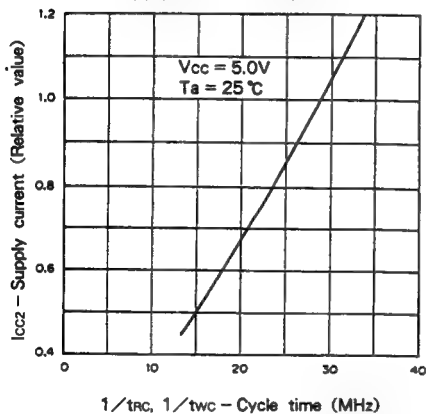
Supply current vs. Supply voltage



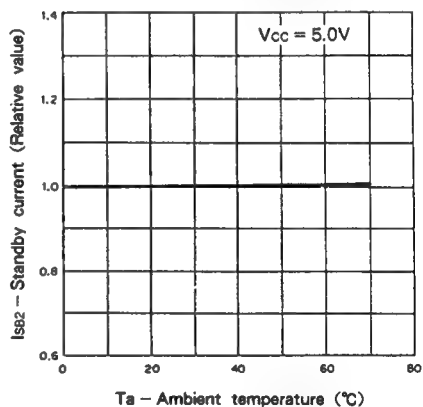
Supply current vs. Ambient temperature



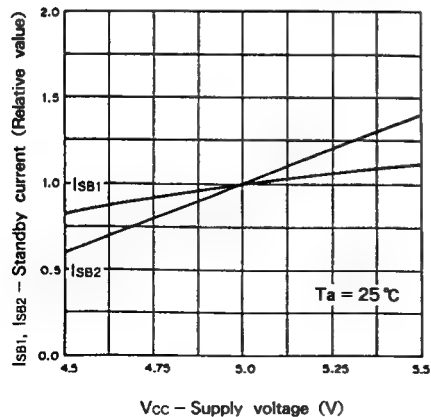
Supply current vs. Cycle time



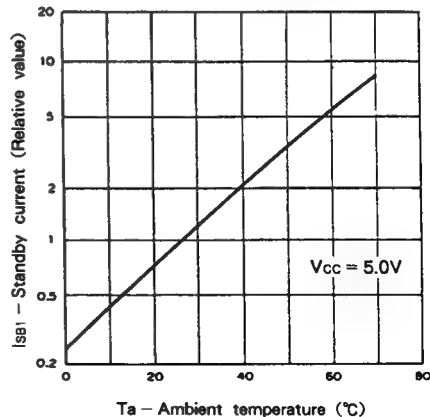
Standby current vs. Ambient temperature



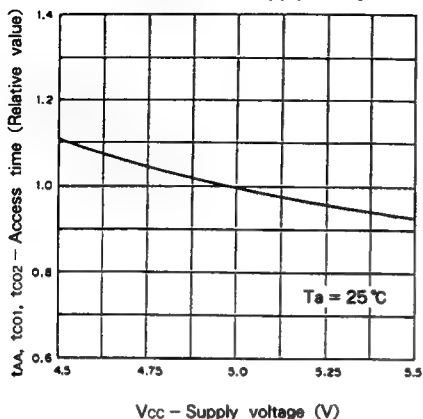
Standby current vs. Supply voltage



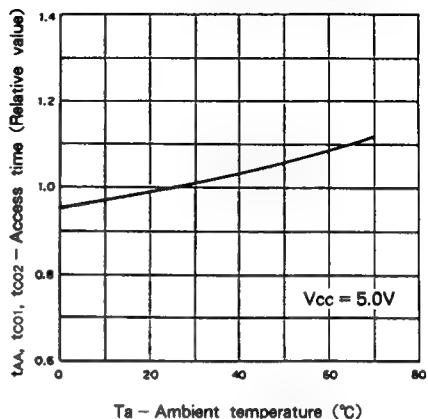
Standby current vs. Ambient temperature



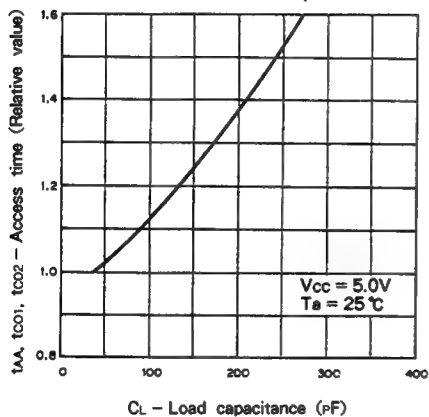
Access time vs. Supply voltage



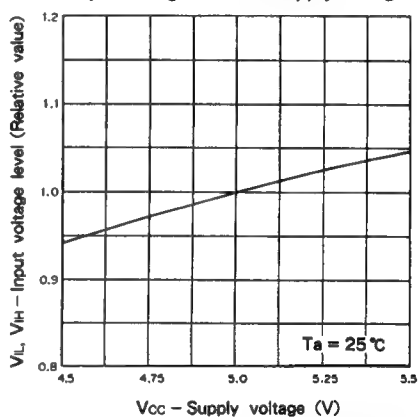
Access time vs. Ambient temperature



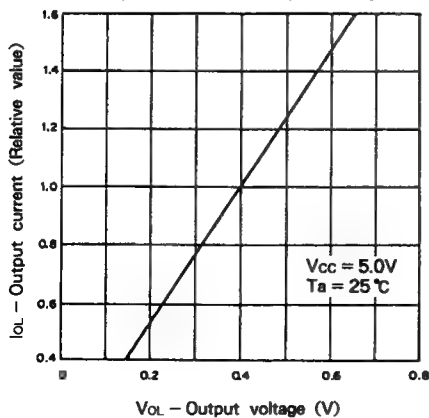
Access time vs. Load capacitance



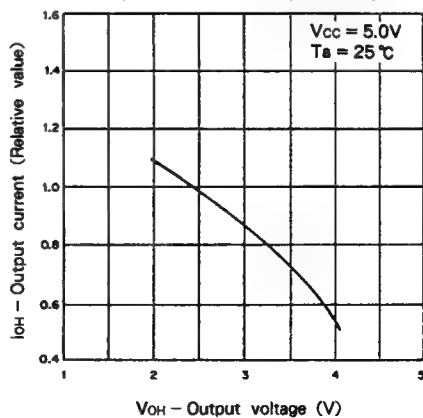
Input voltage level vs. Supply voltage



Output current vs. Output voltage

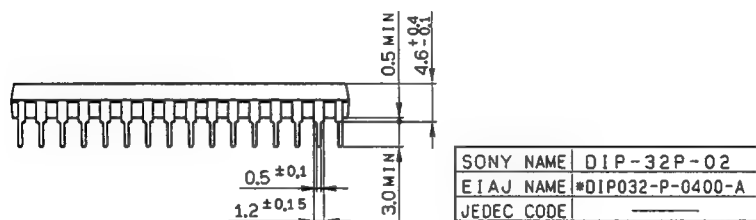
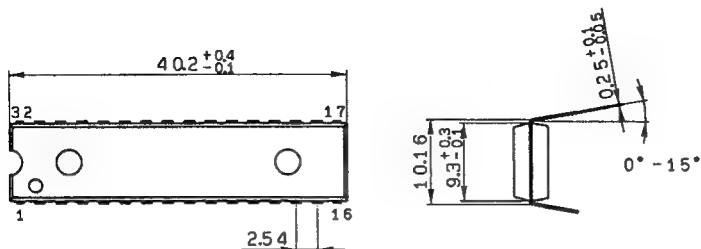


Output current vs. Output voltage

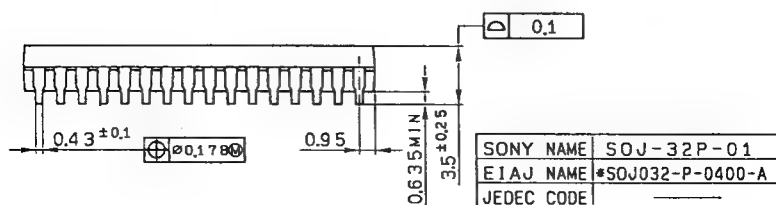
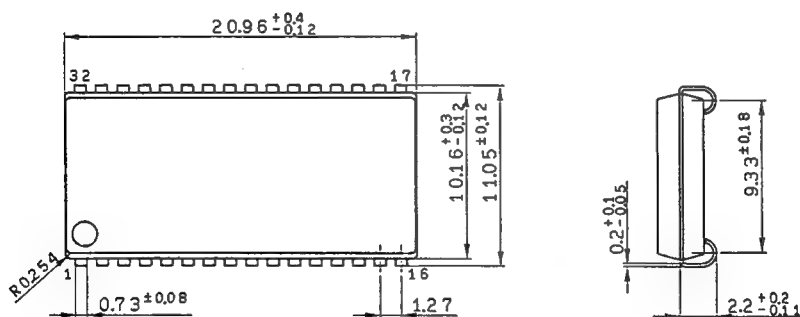


Package Outline Unit : mm

CXK581020SP 32 pin DIP (Plastic) 400mil 3.2g



CXK581020J 32 pin SOJ (Plastic) 400mil 1.3g



SONY**CXK581021J** -47**131,072-word × 8-bit High Speed CMOS Static RAM** *Preliminary***Description**

CXK581021J are 131,072-word × 8-bit high speed CMOS static RAMs suitable for use in high speed and low power applications where battery back up for nonvolatility is required.

Organized as 131,072 words by 8 bits, it operates from a single 5V supply.

Features

- Fast access time : (Access time)
CXK581021J-47 47ns (Max.)
- Low power operation : (Operation)
CXK581021J-47 300mW (Typ. Cycle=Min.)
- Single +5V supply : +5V ± 10%
- Fully static memory ... No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible : All inputs and outputs.
- Available in 32 pin 400-mil SOJ

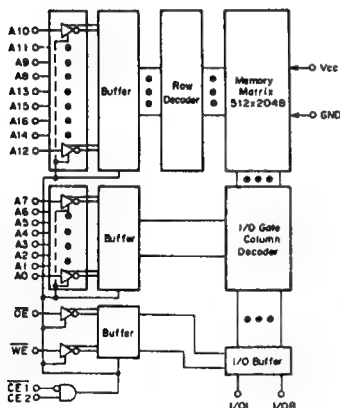
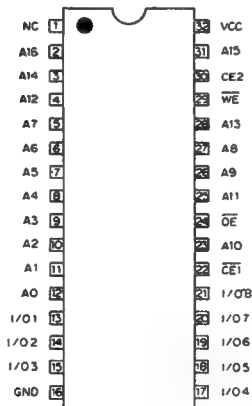
32 pin SOJ (Plastic)

**Function**

131,072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration**
(Top View)**Pin Description**

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 * to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	260•10	°C •sec

* V_{CC}, V_{IN}, V_{I/O}=-3.5V Min. for pulse width less than 20ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC2}
L	H	L	H	Read	Data out	I _{CC2}
L	H	X	L	Write	Data in	I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL}=-3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions	Min.	Typ. *	Max.	Unit
Input leakage current	I _{II}	V _{IN} =GND to V _{CC}	-2	—	2	μA
Output leakage current	I _{LO}	V _{I/O} =GND to V _{CC} , $\overline{CE1}=V_{IH}$ or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL}	-2	—	2	μA
Operating power supply current	I _{CC1}	$\overline{CE1}=V_{IL}$, CE2=V _{IH} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	—	—	—	mA
Average operating current	I _{CC2}	Cycle=Min., Duty=100%, I _{OUT} =0mA	—	—	130	mA
Standby current	I _{SB1}	$\overline{CE1} \geq V_{CC}-0.2V$ or CE2 ≤ 0.2V, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	—	0.01	2	mA
	I _{SB2}	$\overline{CE1}=V_{IH}$ or CE2=V _{IL} , Cycle=Min.	—	—	55	mA
Output high voltage	V _{OH}	I _{OH} =-4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =8.0mA	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

(T_a=25 °C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	7	pF

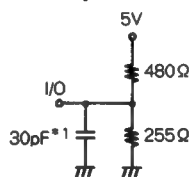
* This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions (V_{CC}=5V ± 10%, T_a=0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} =3.0V
Input pulse low level	V _{IL} =0V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)*2

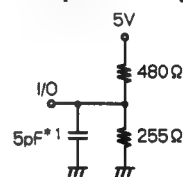
* 1. C_L includes scope and jig capacitances.* 2. For t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	Min.	Max.	Unit
Read cycle time	t _{RC}	47	—	ns
Address access time	t _{AA}	—	47	ns
Chip enable access time ($\overline{\text{CE1}}$)	t _{CO1}	—	47	ns
Chip enable access time (CE2)	t _{CO2}	—	47	ns
Output enable to output valid	t _{OE}	—	25	ns
Output hold from address change	t _{OH}	5	—	ns
Chip enable to output in low Z ($\overline{\text{CE1}}$, CE2)	t _{LZ1} *, t _{LZ2} *	5	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ} *	0	—	ns
Chip disable to output in high Z ($\overline{\text{CE1}}$, CE2)	t _{HZ1} *, t _{HZ2} *	0	20	ns
Output disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	0	20	ns
Chip enable to power up time ($\overline{\text{CE1}}$, CE2)	t _{PU}	0	—	ns
Chip enable to power down time ($\overline{\text{CE1}}$, CE2)	t _{PD}	—	47	ns

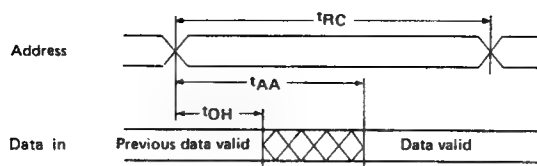
• Write cycle

Item	Symbol	Min.	Max.	Unit
Write cycle time	t _{WC}	47	—	ns
Address valid to end of write	t _{AW}	40	—	ns
Chip enable to end of write	t _{CW}	40	—	ns
Data to write time overlap	t _{DW}	20	—	ns
Data hold from write time	t _{DH}	0	—	ns
Write pulse width	t _{WP}	35	—	ns
Address set up time	t _{AS}	0	—	ns
Write recovery time ($\overline{\text{WE}}$, $\overline{\text{CE1}}$)	t _{WR1}	3	—	ns
Write recovery time (CE2)	t _{WR2}	5	—	ns
Output active from end of write	t _{OW} *	5	—	ns
Write to output in high Z	t _{WHZ} *	0	15	ns

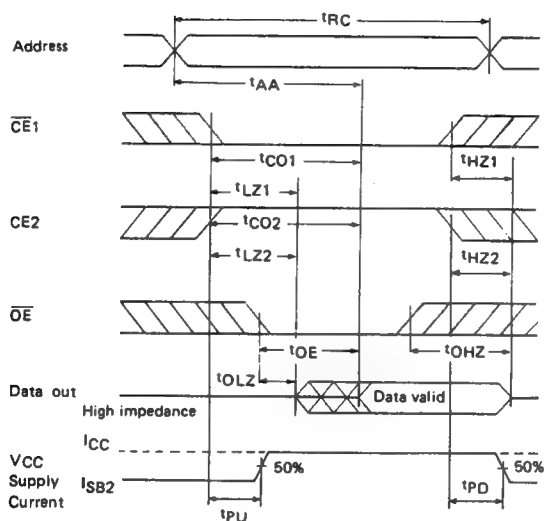
* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1 (2).
This parameter is sampled and not 100% tested.

Timing Waveform

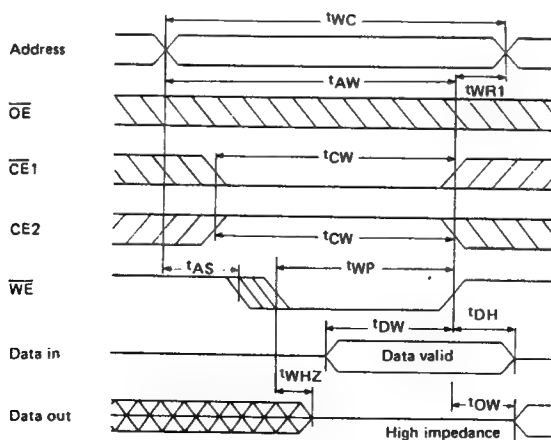
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



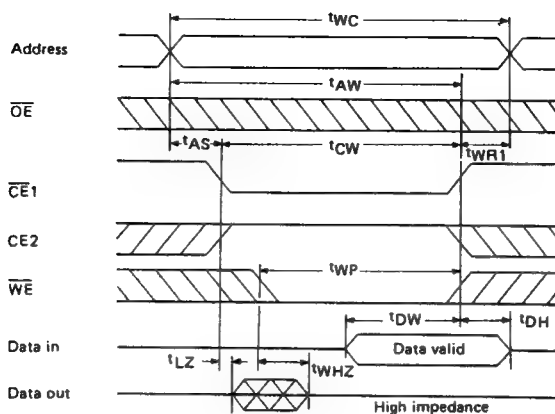
- Read cycle (2) : $\overline{WE} = V_{IH}$



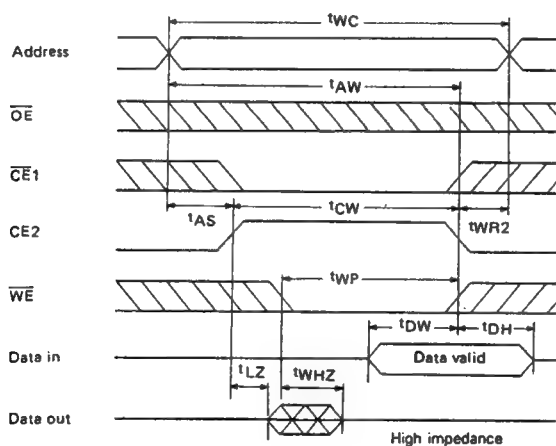
- Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : $\overline{\text{CE2}}$ control



* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

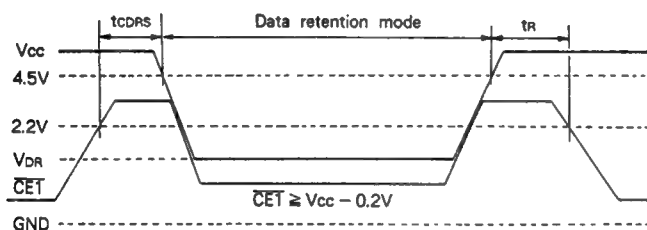
(Ta=0 to 70 °C)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Data retention voltage	V _{DR}	*	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V *	—	—	150	μA
	I _{CCDR2}	V _{CC} =2.0 to 5.5V *	—	0.01	2	mA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t _R		5	—	—	ms

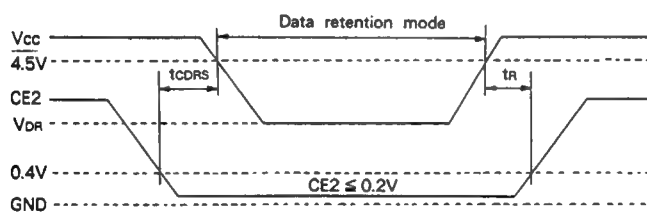
* $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

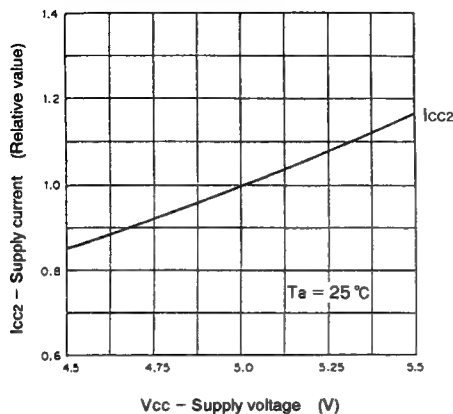


- Low supply voltage data retention waveform (2) ($CE2$ control)

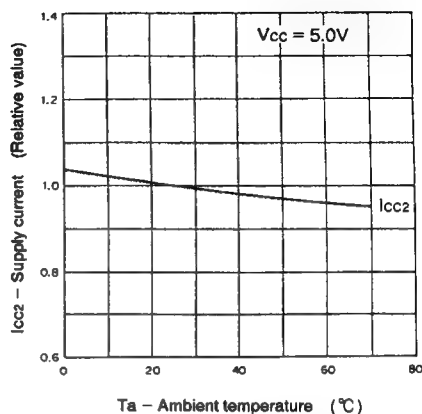


Example of Representative Characteristics

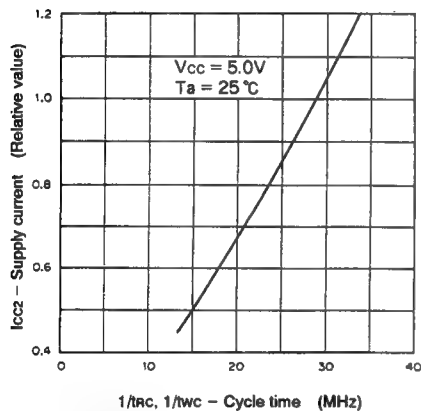
Supply current vs. Supply voltage



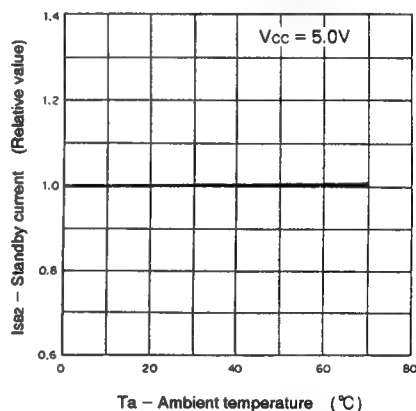
Supply current vs. Ambient temperature



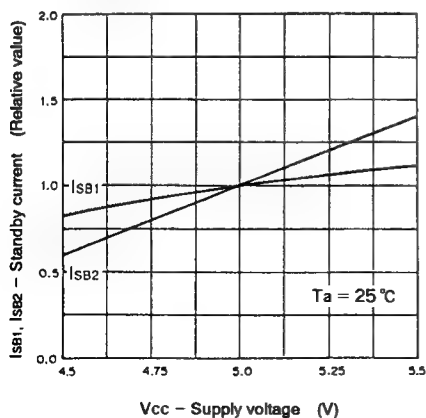
Supply current vs. Cycle time



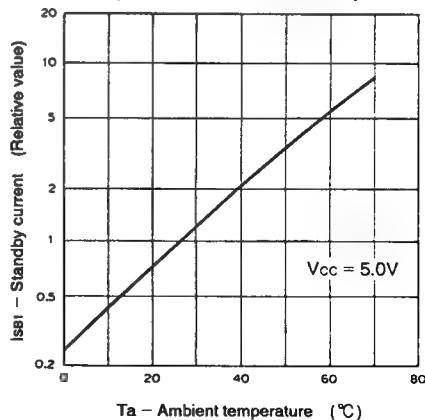
Standby current vs. Ambient temperature



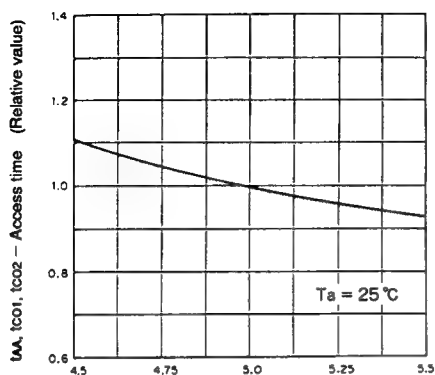
Standby current vs. Supply voltage



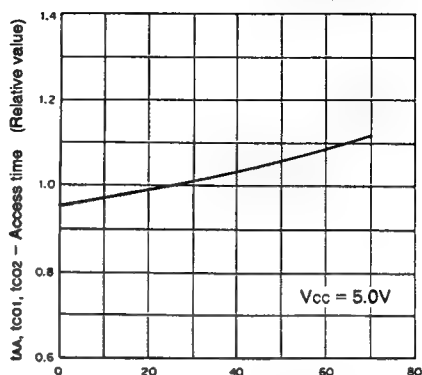
Standby current vs. Ambient temperature



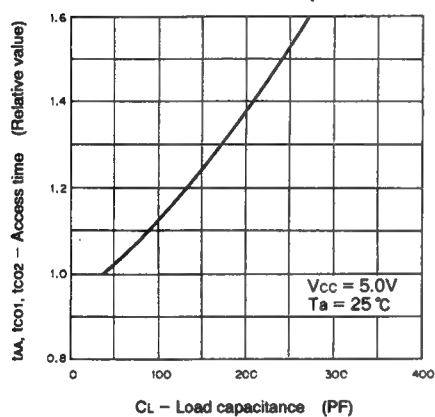
Access time vs. Supply voltage



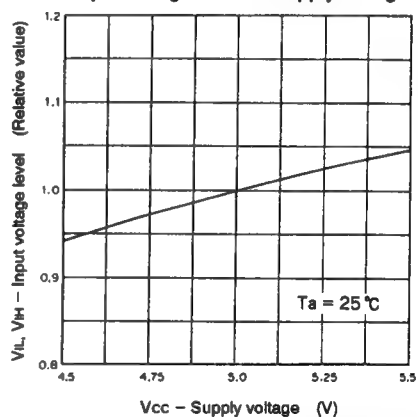
Access time vs. Ambient temperature



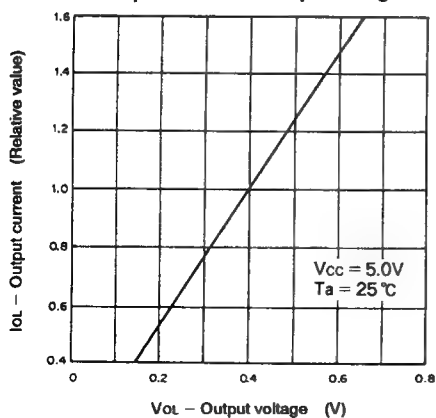
Access time vs. Load capacitance



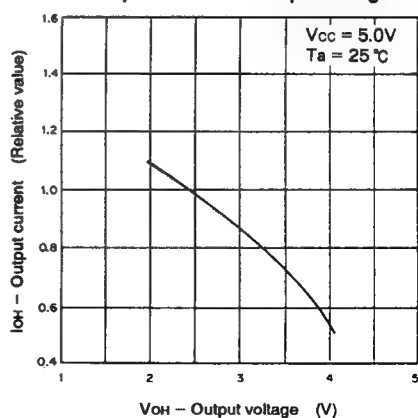
Input voltage level vs. Supply voltage



Output current vs. Output voltage

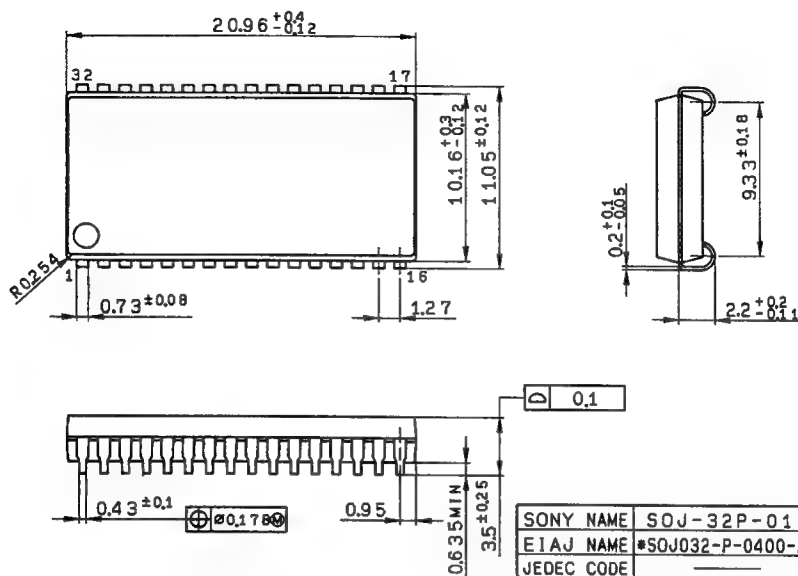


Output current vs. Output voltage



Package Outline Unit : mm

32pin SOJ (Plastic) 400mil 1.3g



SONY**CXK581120J** -15/17/20**131,072-word × 8-bit High Speed CMOS Static RAM** *Preliminary***Description**

CXK581120J is a high speed 1M-bit CMOS static RAM organized as 131,072-words × 8bits. It operates at 15/17/20ns access time from a single 5V power supply, utilizing center-ground/power pin architecture.

Features

- Fast access time : (Access time)
 CXK581120J-15 15ns (Max.)
 CXK581120J-17 17ns (Max.)
 CXK581120J-20 20ns (Max.)
- Low power consumption:
 CXK581120J-15 550mW (Typ., Cycle=Min.)
 CXK581120J-17 500mW (Typ., Cycle=Min.)
 CXK581120J-20 475mW (Typ., Cycle=Min.)
- Single +5V supply :
 CXK581120J-15/17 5V±5%
 CXK581120J-20 5V±10%
- Fully static memory ... No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible: All inputs and outputs.
- Available in 32 pin SOJ package.

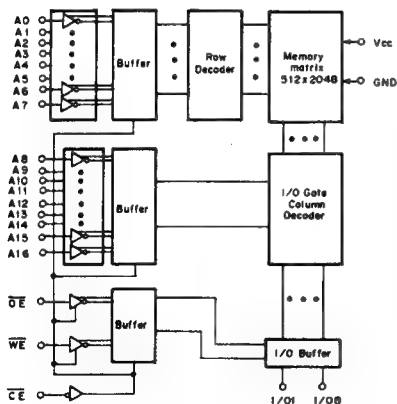
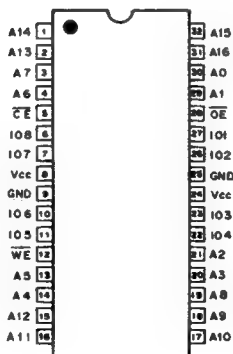
32 pin SOJ (Plastic)

**Function**

131,072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration**
(Top View)**Pin Description**

Symbol	Description
A0 to A16	Address Input
I/O1 to I/O8	Data input/output
\overline{CE}	Chip enable input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 to V _{CC} +0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O8	V _{CC} current
H	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC}
L	L	H	Read	Data out	I _{CC}
L	x	L	Write	Data in	I _{CC}

x : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	-15/17	V _{CC}	4.75	5.0	5.25	V
	-20		4.5	5.0	5.5	V
Input high voltage		V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage		V _{IL}	-0.3	—	0.8	V

Electrical Characteristics

• DC and operating characteristics

Item	Symbol	Test conditions	Min.	Typ. *	Max.	Unit
Input leakage current	I_{LI}	$V_{IN}=GND$ to V_{CC}	-1	—	1	μA
Output leakage current	I_{LO}	$V_{IO}=GND$ to V_{CC} , $CE=V_{IH}$ or $OE=V_{IH}$ or $\overline{WE}=V_{IL}$	-1	—	1	μA
Average operating current	I_{CC}	Cycle=Min., Duty=100%, $I_{OUT}=0mA$ $CE=V_{IL}$ $V_{IN}=V_{IH}$ or V_{IL}	-15	—	110	mA
			-17	—	100	
			-20	—	95	
Standby current	I_{SB1}	$\overline{CE} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	—	—	1	mA
	I_{SB2}	Cycle=Min., Duty=100%, $CE=V_{IH}$, $V_{IN}=V_{IL}$ or V_{IH}	—	30	40	mA
Output high voltage	V_{OH}	$I_{OH}=-4.0mA$	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL}=8.0mA$	—	—	0.4	V

* $V_{CC}=5V$, $T_a=25^\circ C$

I/O Capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN}=0V$	—	6	pF
I/O capacitance	C_{IO}	$V_{IO}=0V$	—	7	pF

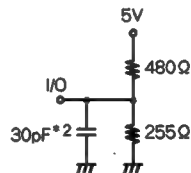
* This parameter is sampled and is not 100% tested.

AC Characteristics

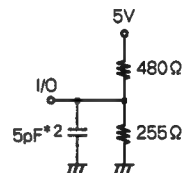
• AC test conditions ($V_{CC}=5V \pm 5\%$ *1, $T_a=0$ to $+70^\circ C$)

Item	Conditions
Input pulse high level	$V_{IH}=3.0V$
Input pulse low level	$V_{IL}=0V$
Input rise time	$t_r=3ns$
Input fall time	$t_f=3ns$
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*3



- * 1. $V_{CC}=5V \pm 10\%$ for CXK581120J-20
- * 2. Including scope and jig capacitance.
- * 3. For t_{LZ} , t_{HZ} , t_{OLZ} , t_{OLH} , t_{OW} , t_{WHZ} .

Fig. 1

• Read cycle

Item	Symbol	-15		-17		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	15	—	17	—	20	—	ns
Address access time	t _{AA}	—	15	—	17	—	20	ns
Chip enable access time	t _{CO}	—	15	—	17	—	20	ns
Output enable to output valid	t _{OE}	—	8	—	9	—	10	ns
Output hold from address change	t _{OH}	2	—	3	—	3	—	ns
Chip enable to output in low Z (\overline{CE})	t _{LZ} *	3	—	3	—	3	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ} *	2	—	2	—	2	—	ns
Chip disable to output in high Z (\overline{CE})	t _{HZ} *	—	6	—	7	—	8	ns
Output disable to output in high Z (\overline{OE})	t _{OHZ} *	—	6	—	7	—	8	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip enable to power down time	t _{PD}	—	15	—	17	—	20	ns

• Write cycle

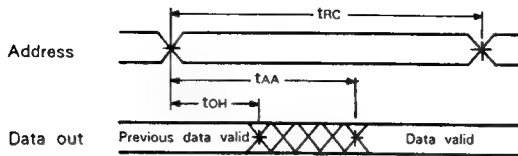
Item	Symbol	-15		-17		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	15	—	17	—	20	—	ns
Address valid to end of write	t _{AW}	12	—	13	—	15	—	ns
Chip enable to end of write	t _{CW}	12	—	13	—	15	—	ns
Data to write time overlap	t _{DW}	10	—	10	—	12	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	12	—	13	—	15	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	3	—	3	—	3	—	ns
Write to output in high Z	t _{WHZ} *	—	8	—	9	—	9	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1 (2).

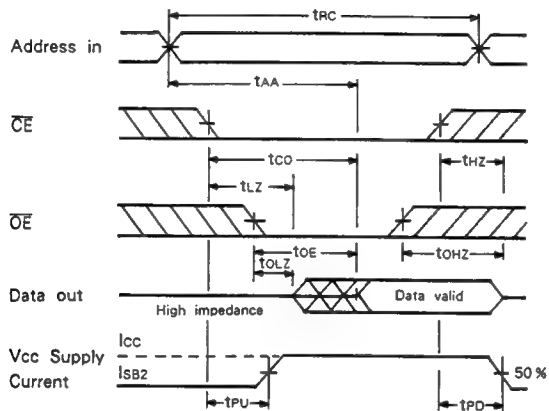
This parameter is sampled and not 100% tested.

Timing Waveform

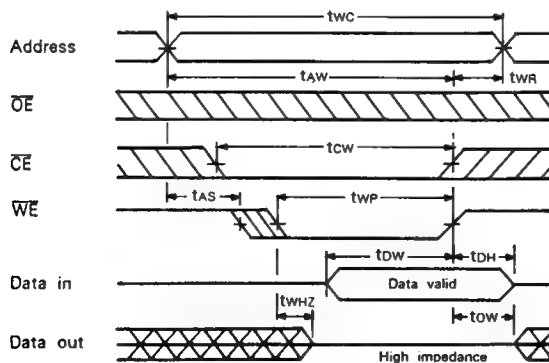
- Read cycle (1) : $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



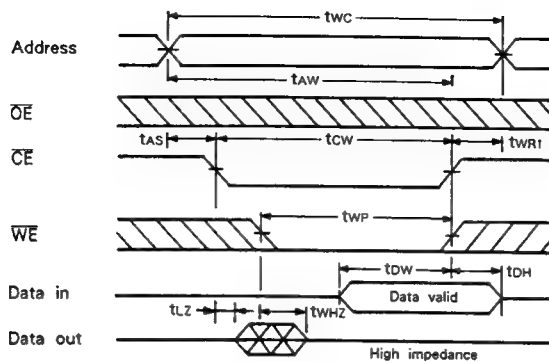
- Read cycle (2) : $\overline{WE}=V_{IH}$



- Write cycle (1) : \overline{WE} control



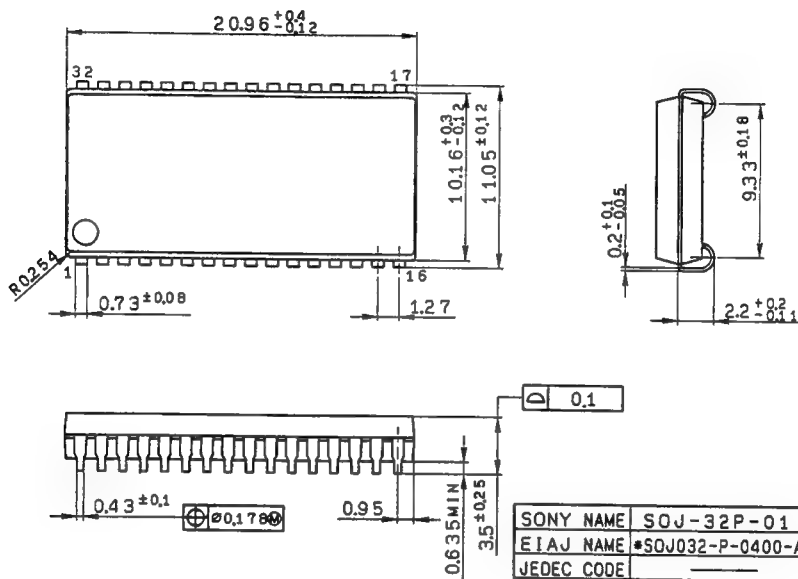
• Write cycle (2) : \overline{CE} control



- *1 Write occurs during the low overlap of \overline{CE} and \overline{WE} .
- *2 During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

32pin SOJ (Plastic) 400mil 1.3g



SONY CXK584000TM/YM/M/P -55L/70L/85L/10L -55LL/70LL/85LL/10LL

524288-word × 8-bit High Speed CMOS Static RAM

Preliminary

Description

CXK584000TM/YM/M/P is a 4,194,304 bits high speed CMOS static RAM organized as 524,288 words by 8-bits. Polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability. Operating on a single 2.7 to 5.5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

Features

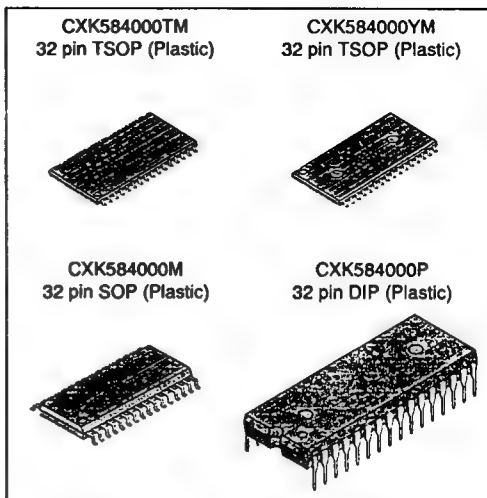
- Wide supply voltage range: 2.7 to 5.5V
- Fast access time: 5V operation/3V operation

-55L/55LL	55ns/110ns (Max.)
-70L/70LL	70ns/140ns (Max.)
-85L/85LL	85ns/170ns (Max.)
-10L/10LL	100ns/200ns (Max.)
- Low stand-by current:

-55L/70L/85L/10L	100 μ A (Max.)
-55LL/70LL/85LL/10LL	50 μ A (Max.)
- Low data retention current:

-55L/70L/85L/10L	15 μ A (Max.) Ta=0 to +40 °C
-55LL/70LL/85LL/10LL	3 μ A (Max.) Ta=0 to +40 °C
- Low voltage data retention: 2.0V (Min.)
- Package line-up

CXK584000TM/YM	400mil 32 pin TSOP (Type II)
CXK584000M	525mil 32 pin SOP
CXK584000P	600mil 32 pin DIP



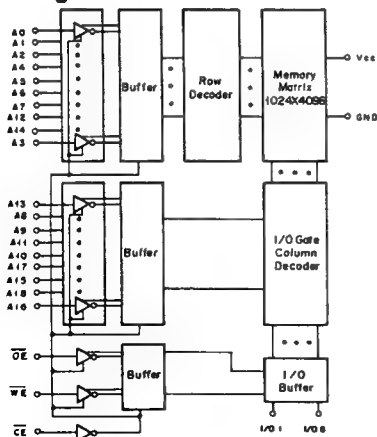
Function

524288-word × 8-bit static RAM

Structure

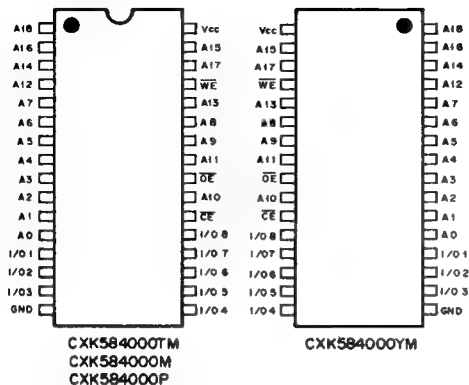
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A18	Address input
I/O1 to I/O8	Data input/output
\overline{CE}	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to Vcc+0.5	V
Input and output voltage	V _{IO}	-0.5 * to Vcc+0.5	V
Allowable power dissipation	P _d	CXK584000TM/YM/M	0.7
		CXK584000P	1.0
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature * time	T _{solder}	CXK584000TM/YM	235 * 10
		CXK584000M/P	260 * 10

* V_{IN}, V_{IO}=-3.0V Min. for pulse width less than 50ns.

Truth Table

\overline{CE}	OE	WE	Mode	I/O pin	Vcc current
H	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	x	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

x : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Vcc=5V ± 10%			Vcc=2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	Vcc	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V _{IH}	2.2	—	Vcc+0.3	2.2	—	Vcc+0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	-0.3 *	—	0.4	V

* V_{IL} = -3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions		Vcc=5V ± 10%			Vcc=3V ± 10%			Unit
				Min.	Typ. *1	Max.	Min.	Typ. *2	Max.	
Input leakage current	I _{LI}	V _{IH} =GND to Vcc		-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{IO} =GND to Vcc		-1	—	1	-1	—	1	μA
Operating power supply current	I _{CC1}	$\overline{CE}=V_{IL}$, V _{IH} =V _{IH} or V _{IL} I _{OUT} =0mA		—	6	15	—	0.4	0.8	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA		—	60	100	—	20	35	mA
	I _{CC3}	Cycle time 1 μs Duty=100% I _{OUT} =0mA CE ≤ 0.2V, V _{IL} ≤ 0.2V, V _{IH} ≥ Vcc-0.2V		—	10	20	—	5	10	mA
Standby current	I _{SB1}	$\overline{CE} \geq Vcc-0.2V$	L *3	0 to +70°C	—	—	100	—	—	74
				0 to +40°C	—	—	35	—	—	24
				+25°C	—	2	—	1	—	—
			LL *4	0 to +70°C	—	—	50	—	—	22
				0 to +40°C	—	—	18	—	—	4.5
				+25°C	—	2	—	0.5	—	—
	I _{SB2}	$\overline{CE}=V_{IH}$		—	0.3	3	—	0.06	0.3	mA
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.4	—	—	2.2	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

*1 Vcc=5V, Ta=25°C

*2 Vcc=3V, Ta=25°C

*3 Guaranteed for L-version (-55L/70L/85L/10L)

*4 Guaranteed for LL-version (-55LL/70LL/85LL/10LL)

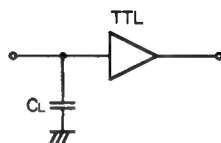
I/O Capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.**AC Characteristics****● AC test conditions**(V_{CC}=2.7 to 5.5V, Ta=0 to +70°C)

Item		Conditions	
		V _{CC} =5V	V _{CC} =3V
Input pulse high level		V _{IH} =2.2V	V _{IH} =2.2V
Input pulse low level		V _{IL} =0.8V	V _{IL} =0.4V
Input rise time		t _r =5ns	t _r =5ns
Input fall time		t _f =5ns	t _f =5ns
Input and output reference level		1.5V	1.5V
Output load conditions	-70L/70LL	C _L * =100pF, 1TTL	C _L * =100pF, 1TTL
	-85L/85LL		
	-10L/10LL	C _L * =30pF, 1TTL	C _L * =30pF, 1TTL
	-55L/55LL		

* C_L includes scope and jig capacitances.

• Read cycle

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	- 55L/55LL		- 70L/70LL		- 85L/85LL		- 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	55	—	70	—	85	—	100	—	ns
Address access time	t _{AA}	—	55	—	70	—	85	—	100	ns
Chip enable access time	t _{CO}	—	55	—	70	—	85	—	100	ns
Output enable to output valid	t _{OE}	—	30	—	40	—	45	—	50	ns
Output hold from address change	t _{OH}	10	—	10	—	10	—	10	—	ns
Chip enable to output in low Z (\overline{CE})	t _{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z (\overline{CE})	t _{HZ} *	0	20	0	25	0	30	0	35	ns
Output disable to output in high Z (\overline{OE})	t _{OHZ} *	0	20	0	25	0	30	0	35	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	- 55L/55LL		- 70L/70LL		- 85L/85LL		- 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	55	—	70	—	85	—	100	—	ns
Address valid to end of write	t _{AW}	50	—	60	—	70	—	80	—	ns
Chip enable to end of write	t _{CW}	50	—	60	—	70	—	80	—	ns
Data to write time overlap	t _{DW}	25	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	40	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (\overline{CE})	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	5	—	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	20	0	25	0	30	0	30	ns

* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

• Read cycle

(Vcc=3V ± 10%, GND=0V, Ta=0 to +70 °C)

Item	Symbol	- 55L/55LL		- 70L/70LL		- 85L/85LL		- 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	110	—	140	—	170	—	200	—	ns
Address access time	t _{AA}	—	110	—	140	—	170	—	200	ns
Chip enable access time	t _{CO}	—	110	—	140	—	170	—	200	ns
Output enable to output valid	t _{OE}	—	60	—	80	—	90	—	100	ns
Output hold from address change	t _{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z (\overline{CE})	t _{LZ}	20	—	20	—	20	—	20	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	10	—	10	—	10	—	10	—	ns
Chip disable to output in high Z (\overline{CE})	t _{HZ} *	0	40	0	50	0	60	0	70	ns
Output disable to output in high Z (\overline{OE})	t _{OHZ} *	0	40	0	50	0	60	0	70	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

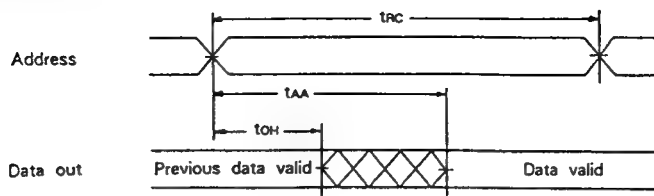
(Vcc=3V ± 10%, GND=0V, Ta=0 to +70 °C)

Item	Symbol	- 55L/55LL		- 70L/70LL		- 85L/85LL		- 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	110	—	140	—	170	—	200	—	ns
Address valid to end of write	t _{AW}	100	—	120	—	140	—	160	—	ns
Chip enable to end of write	t _{CW}	100	—	120	—	140	—	160	—	ns
Data to write time overlap	t _{DW}	50	—	60	—	70	—	80	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	80	—	100	—	120	—	140	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (\overline{CE})	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	40	0	50	0	60	0	60	ns

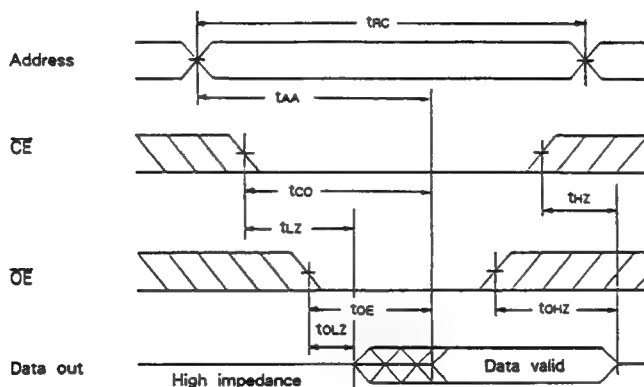
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

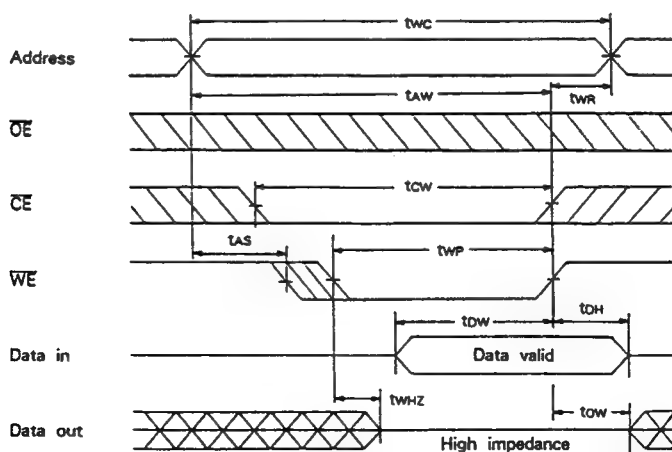
- Read cycle (1) : $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



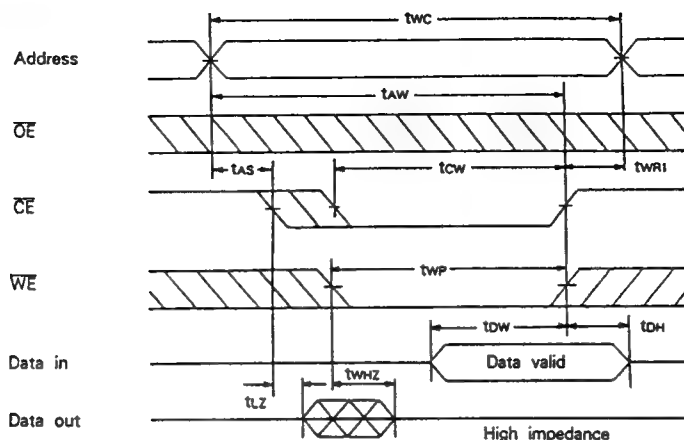
- Read cycle (2) : $\overline{WE}=V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2) : \overline{CE} control



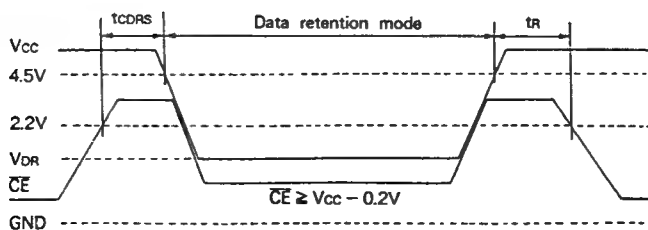
During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

($T_a=0$ to 70°C)

Item	Symbol	Test conditions	- 55L/70L/85L/10L			- 55LL/70LL/85LL/10LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geq V_{CC}-0.2V$	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC}=3.0V$ $\overline{CE} \geq 2.8V$	0 to 70°C		50	—		15	μA
			0 to 40°C		15	—		3	
			25°C		1	—		0.5	
	I_{CCDR2}	$V_{CC}=2.0$ to $5.5V$ $\overline{CE} \geq V_{CC}-0.2V$	—	2	100	—	2	50	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t_R		5	—	—	5	—	—	ms

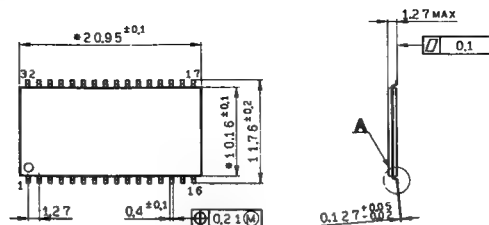
Data retention waveform



Package Outline Unit : mm

CXK584000TM

32pin TSOP (Plastic) 400mil



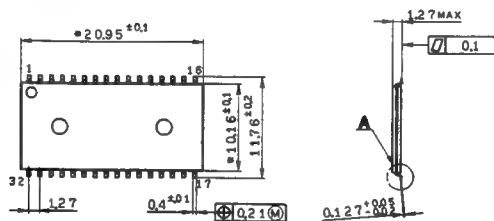
Note) Dimensions marked with *
does not include resin residue.

Detailed diagram of A

SONY NAME	TSOP(I)-32P-L01
EIAJ NAME	TSOP(I)032-P-0400-A
JEDEC CODE	

CXK584000YM

32pin TSOP (Plastic) 400mil



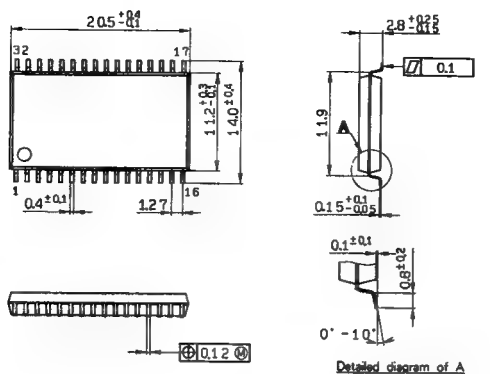
Note) Dimensions marked with *
does not include resin residue.

Detailed diagram of A

SONY NAME	TSOP(I)-32P-L01R
EIAJ NAME	TSOP(I)032-P-0400-B
JEDEC CODE	

CXK584000M

32pin SOP (Plastic) 525mil

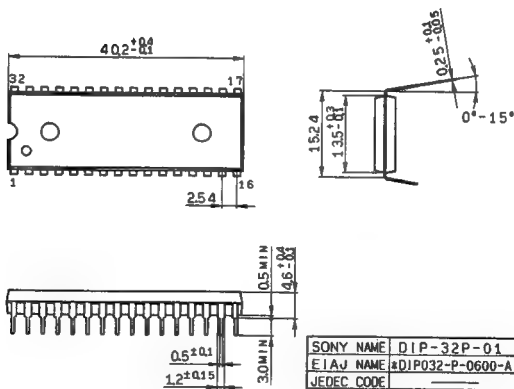


Detailed diagram of A

SONY NAME	SOP-32P-L02
EIAJ NAME	#SOP032-P-0525-A
JEDEC CODE	

CXK584000P

32pin DIP (Plastic) 600mil 4.5g



SONY NAME	DIP-32P-01
EIAJ NAME	#DIP032-P-0600-A
JEDEC CODE	

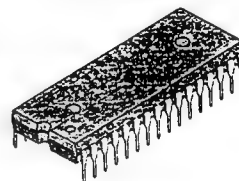
-10L/12L
-10LL/12LL

Preliminary

CXK584001TM/YM/M/P is a **4,194,304** bits high speed CMOS static RAM organized as **524,288** words by 8-bits. Polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability. Operating on a single 3.0V supply, this asynchronous IC is suitable for low voltage microsystems where battery operation is required.

- Single +3V supply: $3V \pm 10\%$
- Fast access time:
 - 10L/10LL 100ns (Max.)
 - 12L/12LL 120ns (Max.)
- Low stand-by current:
 - 10L/12L 1.0 μA (Typ.)
 - 10LL/12LL 0.5 μA (Typ.)
- Low power consumption operation (1MHz):
15mW (Typ.)
- Directly TTL compatible: All inputs and outputs.
- Low voltage data retention: 2.0V (Min.)
- Package line-up

CXK584001TM/YM	400mil 32 pin TSOP (Type II)
CXK584001M	525mil 32 pin SOP
CXK584001P	600mil 32 pin DIP



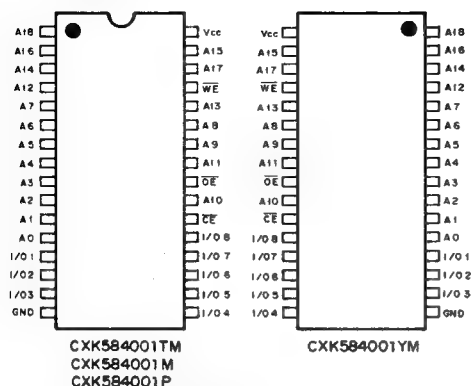
524288-word × 8-bit static RAM

Silicon gate CMOS IC

[illegible]

Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A18	Address input
I/O1 to I/O8	Data input/output
\overline{CE}	Chip enable input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to Vcc+0.5	V
Input and output voltage	V _{I/O}	-0.5 * to Vcc+0.5	V
Allowable power dissipation	P _d	CXK584001TM/YM/M	0.7
		CXK584001P	1.0
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature * time	T _{solder}	CXK584001TM/YM	235 * 10
		CXK584001M/P	260 * 10

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	Mode	I/O pin	Vcc current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	X	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70 °C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	2.7	—	3.3	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(V_{CC}=3V ± 10%, GND=0V, Ta=0 to +70 °C)

Item	Symbol	Test conditions			Min.	Typ.*1	Max.	Unit
Input leakage current	I _I	V _{IN} =GND to V _{CC}			-1	—	1	μA
Output leakage current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{IO} =GND to V _{CC}			-1	—	1	μA
Operating power supply current	I _{CC1}	$\overline{CE}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA			—	0.4	0.8	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA			—	20	40	mA
	I _{CC3}	Cycle time 1 μs Duty=100% I _{OUT} =0mA $\overline{CE} \leq 0.2V$, V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} -0.2V			—	5	10	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$	L*2	0 to +70 °C	—	—	74	μA
				0 to +40 °C	—	—	24	
				+25 °C	—	1	—	
			LL*3	0 to +70 °C	—	—	22	
				0 to +40 °C	—	—	4.5	
				+25 °C	—	0.5	—	
	I _{SB2}	$\overline{CE}=V_{IH}$			—	0.06	0.3	mA
Output high voltage	V _{OH}	I _{OH} =-1.0mA			2.2	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA			—	—	0.4	V

*1 V_{CC}=3V, Ta=25 °C

*2 Guaranteed for L-version (-10L/12L)

*3 Guaranteed for LL-version (-10LL/12LL)

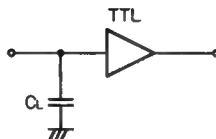
I/O Capacitance

(Ta=25 °C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	8	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	10	pF

Note) This parameter is sampled and is not 100% tested.**AC Characteristics****● AC test conditions**(V_{CC}=3V ± 10%, Ta=0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} =2.2V
Input pulse low level	V _{IL} =0.8V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	C _L * =100pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	– 10L/10LL		– 12L/12LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	100	—	120	—	ns
Address access time	t _{AA}	—	100	—	120	ns
Chip enable access time	t _{CO}	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	50	—	60	ns
Output hold from address change	t _{OH}	10	—	10	—	ns
Chip enable to output in low Z (\overline{CE})	t _{LZ}	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t _{OLZ}	5	—	5	—	ns
Chip disable to output in high Z (\overline{CE})	t _{HZ} *	0	40	0	45	ns
Output disable to output in high Z (\overline{OE})	t _{OHZ} *	0	40	0	45	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

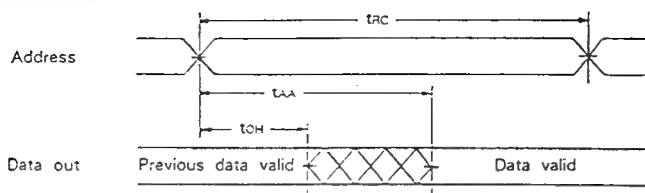
• Write cycle

Item	Symbol	– 10L/10LL		– 12L/12LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	100	—	120	—	ns
Address valid to end of write	t _{AW}	90	—	100	—	ns
Chip enable to end of write	t _{CW}	90	—	100	—	ns
Data to write time overlap	t _{DW}	50	—	55	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	80	—	90	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time (\overline{WE})	t _{WR}	0	—	0	—	ns
Write recovery time (\overline{CE})	t _{WR1}	0	—	0	—	ns
Output active from end of write	t _{OW}	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	40	0	45	ns

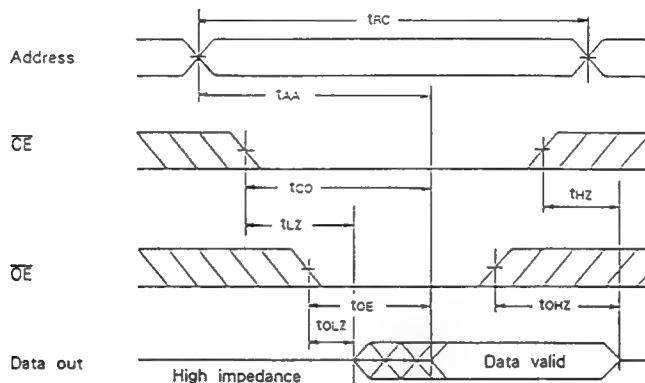
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

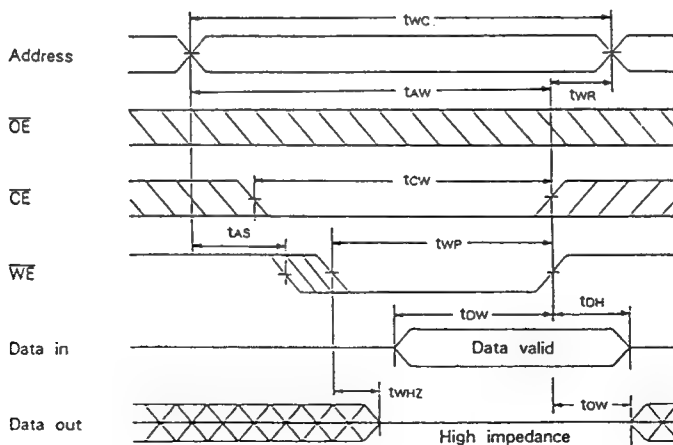
- Read cycle (1) : $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



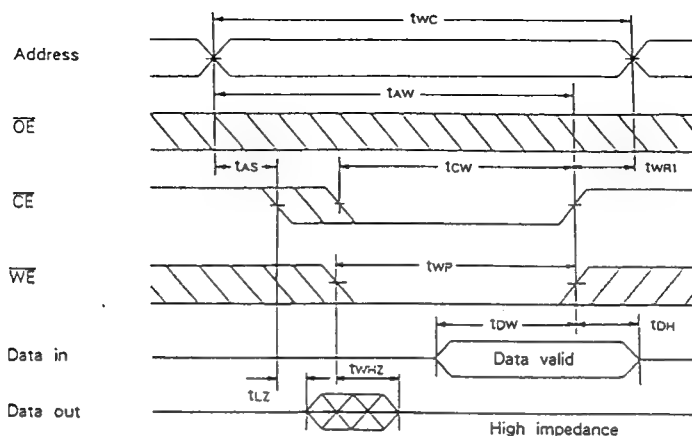
- Read cycle (2) : $\overline{WE}=V_{IH}$



- Write cycle (1) : \overline{WE} control



• Write cycle (2) : \overline{CE} control



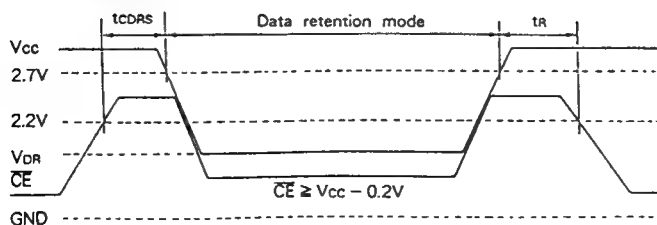
During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

($T_a = 0$ to 70°C)

Item	Symbol	Test conditions	- 10L/12L			- 10LL/12LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	3.3	2.0	—	3.3	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$ $\overline{CE} \geq 2.8V$	0 to 70°C	—	50	—	—	15	μA
			0 to 40°C	—	15	—	—	3	
			25°C	—	1	—	0.5	—	
	I_{CCDR2}	$V_{CC} = 2.0$ to $3.3V$ $\overline{CE} \geq V_{CC} - 0.2V$	—	1	74	—	0.5	22	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t_R		5	—	—	5	—	—	ms

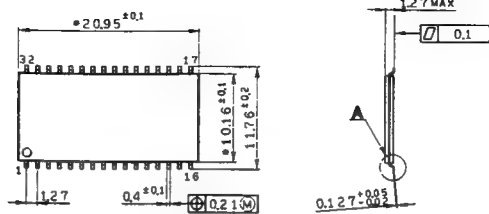
Data retention waveform



Package Outline Unit : mm

CXK584001TM

32pin TSOP (Plastic) 400mil



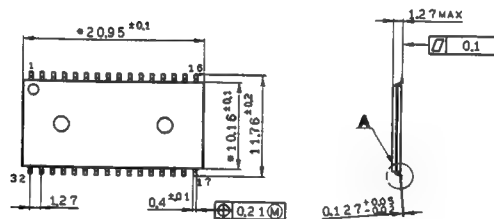
Note) Dimensions marked with *
does not include resin residue.

Detailed diagram of A

SONY NAME	TSOP(II)-32P-L01
EIAJ NAME	TSOP(E)32-P-0400-A
JEDEC CODE	

CXK584001YM

32pin TSOP (Plastic) 400mil



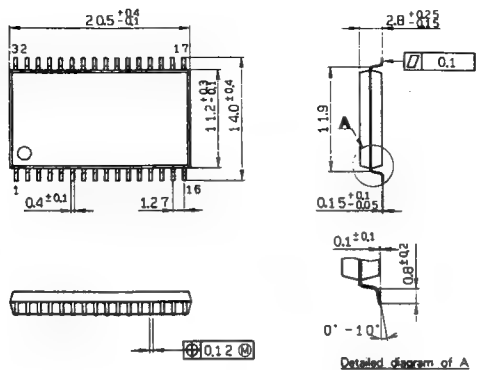
Note) Dimensions marked with *
does not include resin residue.

Detailed diagram of A

SONY NAME	TSOP(II)-32P-L01R
EIAJ NAME	TSOP(E)32-P-0400-B
JEDEC CODE	

CXK584001M

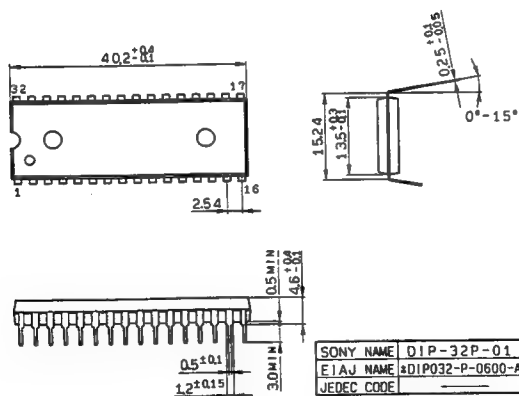
32pin SOP (Plastic) 525mil



SONY NAME	SOP-32P-L02
EIAJ NAME	±SOP032-P-0525-A
JEDEC CODE	

CXK584001P

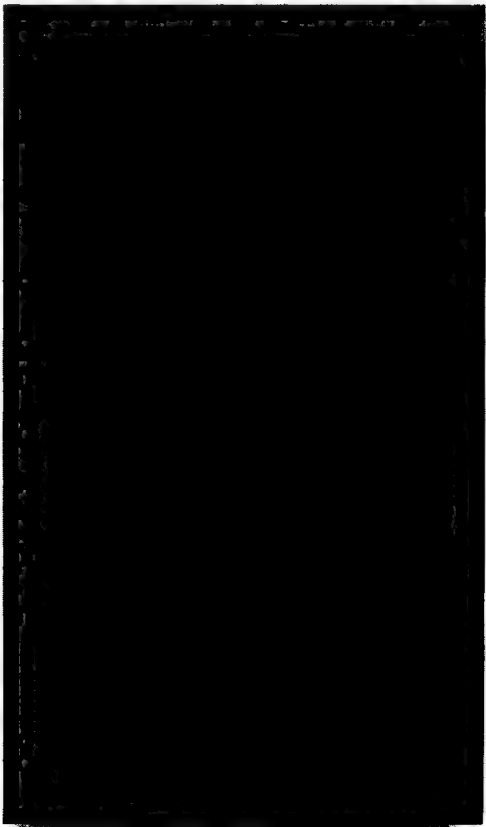
32pin DIP (Plastic) 600mil 4.5q



SONY NAME	DIP-32P-01
EIAJ NAME	±DIP032-P-0600-A
JEDEC CODE	



Application Specific Memories



2) Apprication Specific Memories

Type	Application specific	Functions	Access time	Page
CXK7701J	Cashe memorie	4k × 16bit × 2way	30/35/45ns	351
CXK77910J*		128k × 9bit Self Timed RAM	17/20ns	366

* : under development

High-Speed Latched Cache-SRAM

Description

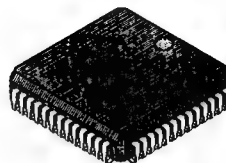
The CXK7701J is a 131,072-bit high speed latched Cache-SRAM suitable for use in high speed cache configurations and low power applications.

Organized as 8192 word \times 16-bit or 4096 word \times 16-bit \times 2 WAY selected by mode control pin, it operates from a single 5V supply.

Features

- Best fit for Cache configurations
Intel 82385 Cache Controller (for 80386-33 MHz, 25MHz, 20MHz)
- Fast access time : (Access time)
CXK7701J-30 30ns (Max.)
CXK7701J-35 35ns (Max.)
CXK7701J-45 45ns (Max.)
- Fast output Enable
CXK7701J-30 10ns (Max.)
CXK7701J-35 13ns (Max.)
CXK7701J-45 16ns (Max.)
- Available in 52 pin PLCC
- Internal 12-bit address latch (A0 – A11)
- Directly TTL compatible : All inputs and outputs

52 pin PLCC (Plastic)

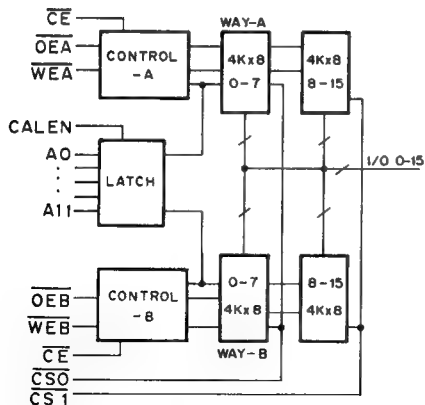


Structure

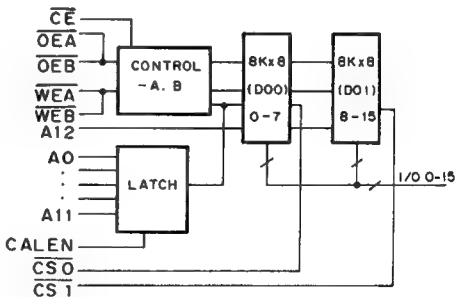
Silicon gate CMOS IC

Block Diagram

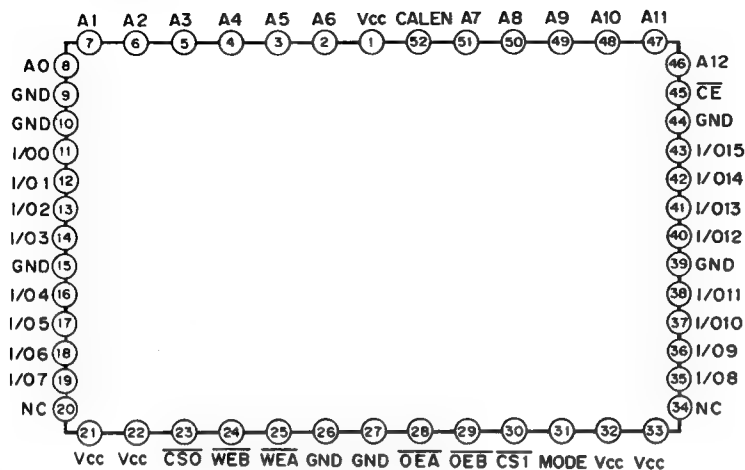
• 2 WAY SET ASSOCIATIVE (MODE = "High")



• DIRECT MAP (MODE = "Low")



Pin Configuration



Pin Description

Symbol	Description
A0 to A12	Address Input
I/O0 to I/O15	Data Input Output
\overline{CE}	Global Chip Enable Input
$\overline{CS0}$, $\overline{CS1}$	Chip Enable Input for I/O 0-7, I/O 8-15
\overline{OEA} , \overline{OEB}	Output Enable Input for Bank-A, Bank-B
\overline{WEA} , \overline{WEB}	Write Enable Input for Bank-A, Bank-B
CALEN	Address Latch Enable Input
MODE	Mode Control
Vcc	+5V Power Supply
GND	Ground
NC	No Connection

Absolute Maximum Ratings

(Ta = 25 °C, GND = 0V)

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	- 0.5*to + 7.0	V
Input Voltage	V _{IN}	- 0.5*to Vcc + 0.5	V
Input & Output Voltage	V _{I/O}	- 0.5*to Vcc + 0.5	V
Power Dissipation	P _D	2.5	W
Operating Temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering Temperature	T _{solder}	260 • 10	°C • sec

*Note) Vcc, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.

DC Recommended Operating Conditions (Ta = 0 to + 70 °C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	Vcc + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

*Note) V_{IL} = - 3.0V Min. for pulse width less than 20ns.

DC and Operating Characteristics

(Vcc = 5V ± 10 %, GND = 0V, Ta = 0 to + 70 °C)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input Leakage Current	I _{LI}	V _{IN} = GND to Vcc	- 2	2	μA
Output Leakage Current	I _{LO}	V _{I/O} = GND to Vcc, \overline{CE} = V _{IH} or $\overline{CS0}$, $\overline{CS1}$ = V _{IH} or \overline{OE} , \overline{OE} = V _{IH} or \overline{WE} , \overline{WE} = V _{IL}	- 2	2	μA
Operating Supply Current	I _{cc1}	$\overline{CS0}$, $\overline{CS1}$ & \overline{CE} = V _{IL} V _{IN} = V _{IL} or V _{IH} I _{OUT} = 0mA	—	180	mA
Average Operating Current	I _{cc2}	100 % Duty Cycle V _{IN} = GND to Vcc I _{OUT} = 0mA	—	240	mA
	I _{cc3}	50 % Duty Cycle V _{IN} = GND to Vcc I _{OUT} = 0mA	—	220	mA
Output High Voltage	V _{OH}	I _{OH} = - 1.0mA	2.4	—	V
Output Low Voltage	V _{OL}	I _{OL} = 4.0mA	—	0.4	V

A. C. Test Condition (Applies to Read & Write Cycle Timing)

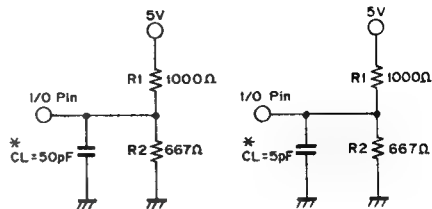
(Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions	Unit
Input Pulse High Level	V _{IH} = 3.0	V
Input Pulse Low Level	V _{IL} = 0.0	V
Input Rise Time	tr = 3	ns
Input Fall Time	tf = 3	ns
Input and Output Reference Level	1.5	V
Output Load (See Test Circuit Fig-1)	R1 1000	Ω
	R2 667	Ω
	CL 50	pF

Fig-1

Output Load (1)

Output Load (2) **



* Including scope and jig capacitance

** For tLZ, tHZ, tOHZ, tOLZ, tWLZ, tWHZ

Truth Tables**Two-Way Mode (Mode = High)**

CE	CS0	CS1	OE _A	OE _B	WE _A	WE _B	Operation
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled
X	X	X	H	H	X	X	Outputs High-Z
X	X	X	L	L	X	X	Outputs High-Z
L	L	H	L	H	H	H	Read I/O 0-7 Way A
L	L	H	H	L	H	H	Read I/O 0-7 Way B
L	H	L	L	H	H	H	Read I/O 8-15 Way A
L	H	L	H	L	H	H	Read I/O 8-15 Way B
L	L	L	L	H	H	H	Read I/O 0-15 Way A
L	L	L	H	L	H	H	Read I/O 0-15 Way B
L	L	H	X	X	L	H	Write I/O 0-7 Way A
L	L	H	X	X	H	L	Write I/O 0-7 Way B
L	H	L	X	X	L	H	Write I/O 8-15 Way A
L	H	L	X	X	H	L	Write I/O 8-15 Way B
L	L	L	X	X	L	H	Write I/O 0-15 Way A
L	L	L	X	X	H	L	Write I/O 0-15 Way B
L	L	H	X	X	L	L	Write I/O 0-7 Way A & B
L	H	L	X	X	L	L	Write I/O 8-15 Way A & B
L	L	L	X	X	L	L	Write I/O 0-15 Way A & B

Note) X: "H" or "L"

Truth Tables

Direct Mode (Mode = Low)

\overline{CE}	$\overline{CS0}$	$\overline{CS1}$	\overline{OEA}	\overline{OEB}	\overline{WEA}	\overline{WEB}	Operation
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled
X	X	X	H	H	X	X	Outputs High-Z
L	L	H	L	L	H	H	Read I/O 0 – 7
L	H	L	L	L	H	H	Read I/O 8 – 15
L	L	L	L	L	H	H	Read I/O 0 – 15
L	L	H	X	X	L	L	Write I/O 0 – 7
L	H	L	X	X	L	L	Write I/O 8 – 15
L	L	L	X	X	L	L	Write I/O 0 – 15

Note) X: "H" or "L"

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Input/Output capacitance	C _{I/O}	V _{I/O} = 0V	—	9	pF

Note) This parameter is sampled and is not 100% tested.

• Write Cycle Timing

(V_{CC} = 5V ± 10%)

Item	Symbol	- 30		- 35		- 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t _{WC}	30	—	35	—	45	—	ns
Address Valid to End of Write	t _{AW}	20	—	25	—	35	—	ns
A12 Valid to End of Write	t _{A12W}	18	—	22	—	30	—	ns
Chip Select to End of Write	t _{CW}	18	—	22	—	30	—	ns
Data Valid to End of Write	t _{DW}	10	—	12	—	15	—	ns
Data Hold from End of Write	t _{DH}	0	—	0	—	0	—	ns
Write Enable Active to High-Z	t _{WHZ} *	—	15	—	15	—	20	ns
WRITE Enable Inactive to Low-Z	t _{WLZ} *	3	—	3	—	3	—	ns
Write Pulse Width	t _{WP}	18	—	22	—	30	—	ns
$\overline{\text{CE}}$ Pulse Width During Chip Enable Controlled Write	t _{CP}	18	—	22	—	30	—	ns
Address Setup Time	t _{AS}	0	—	0	—	0	—	ns
Write Recovery Time	t _{WR}	0	—	0	—	2	—	ns
Address Latch Enable Pulse Width	t _{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t _{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t _{AHL}	5	—	5	—	5	—	ns

* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1 (2).
This parameter is sampled and is not 100% tested.

• Read Cycle Timing

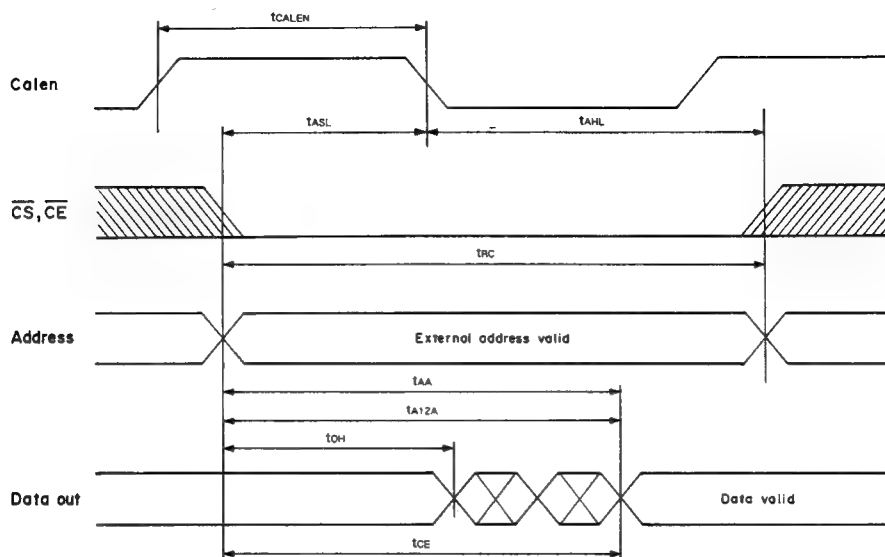
(V_{CC} = 5V ± 10 %)

Item	Symbol	- 30		- 35		- 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t _{RC}	30	—	35	—	45	—	ns
Address Access Time	t _{AA}	—	30	—	35	—	45	ns
A12 Address Access Time	t _{A12A}	—	17	—	25	—	30	ns
Chip Select Access Time	t _{CS} t _{CE}	—	20	—	25	—	35	ns
Output Enable to Output Valid	t _{OE}	—	10	—	13	—	16	ns
Output Hold from Address Change	t _{OH}	3	—	3	—	3	—	ns
Chip Select to Output Low-Z	t _{LZ} *	3	—	3	—	3	—	ns
Output Enable to Output Low-Z	t _{OLZ} *	2	—	2	—	2	—	ns
Chip Deselect to Output High-Z	t _{HZ} *	—	15	—	25	—	30	ns
Output Disable to Output High-Z	t _{OHZ} *	—	10	—	14	—	14	ns
Address Latch Enable Pulse Width	t _{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t _{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t _{AHL}	5	—	5	—	5	—	ns

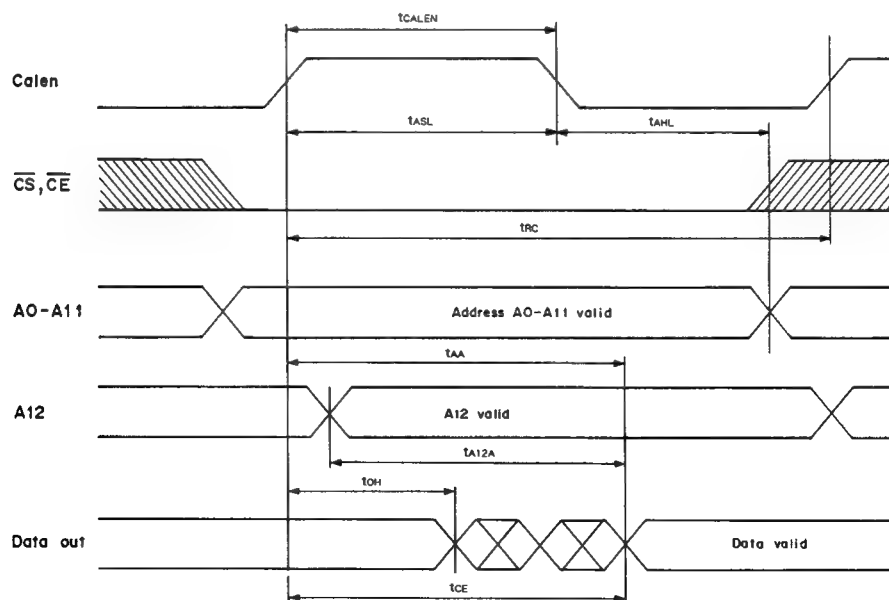
* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1 (2).
This parameter is sampled and is not 100% tested.

Timing Waveform

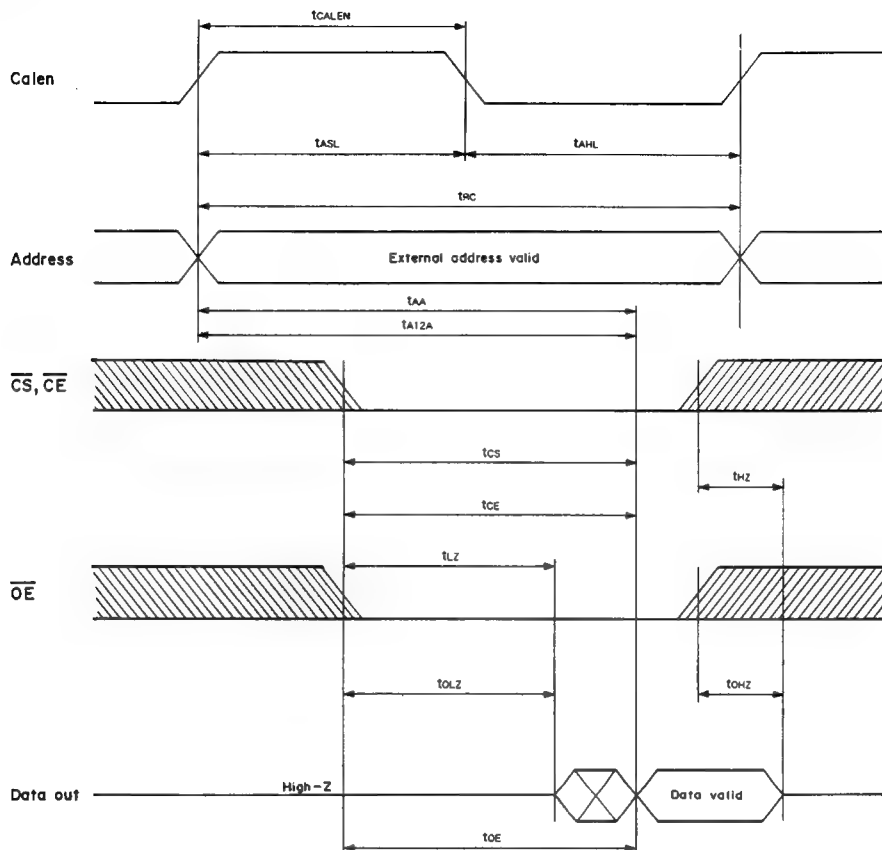
- Read cycle (1) : $\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$, $\overline{CS} = V_{IL}$



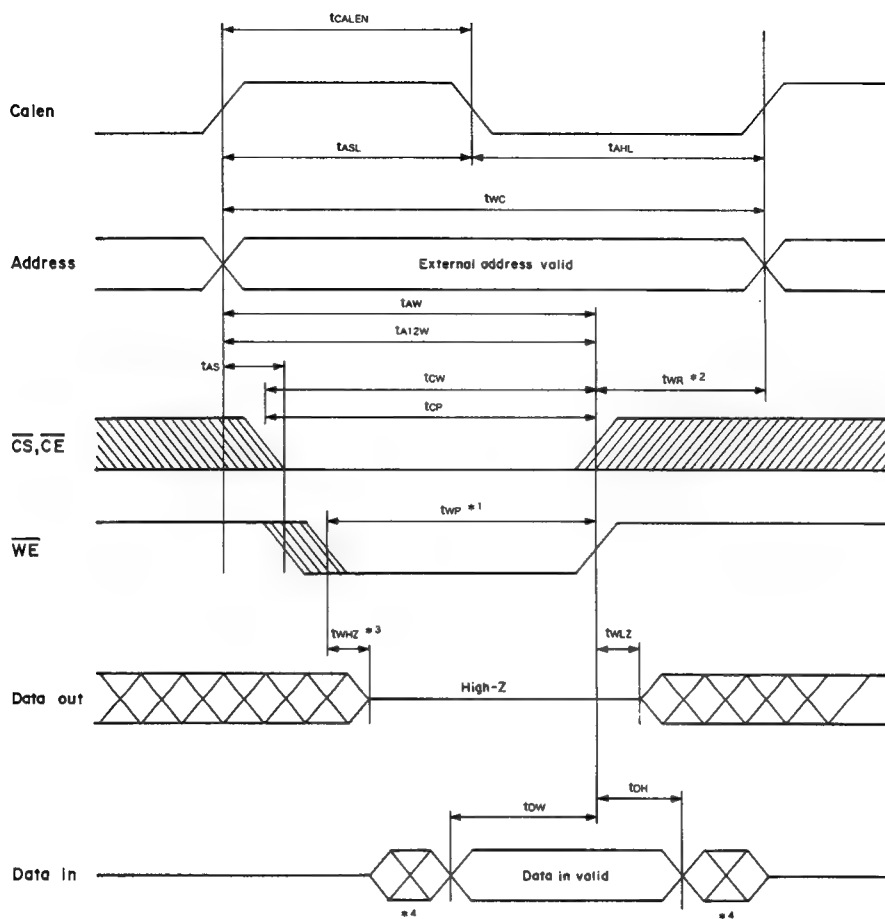
- Read cycle (2) : $\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$, $\overline{CS} = V_{IL}$



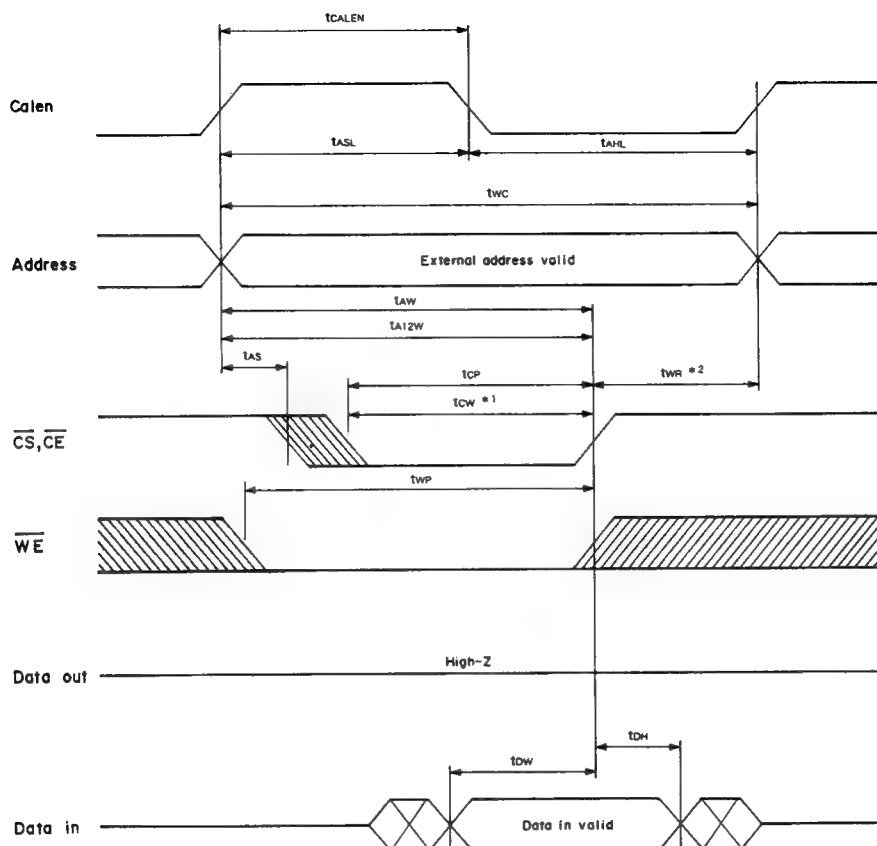
- Read cycle (3) : $\overline{WE} = V_{IH}$



• Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{\text{CE}}$ control



- *1. A write occurs during the low overlap of $\overline{\text{CS}}, \overline{\text{CE}}$ and $\overline{\text{WE}}$.
- *2. t_{WR} is measured from the earlier of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.
- *3. If $\overline{\text{CE}}$ and $\overline{\text{CS}}$ low transition occurs simultaneously with the $\overline{\text{WE}}$ low transition or after the $\overline{\text{WE}}$ transition, output remains in a high impedance state.
- *4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

Control Pin Description

CALEN (Cache Address Latch Enable)

This signal controls the internal address latch that resides between the address inputs and the memory array. When CALEN is high the latch is transparent. The falling edge of CALEN latches the current address inputs.

MODE

This signal controls whether the memory device is to be used in a direct mapped ($8k \times 16$) configuration or a two-way set associative ($2-4k \times 16$) configuration. When the mode signal is high, the device is placed in two-way mode. When the mode pin is low, the device is placed in direct mode.

$\overline{CS0}$, $\overline{CS1}$ (Cache Chip Selects)

These active low signals tie to the cache ram chip selects and individually enable the two bytes of the memory. $\overline{CS0}$ enables bits $1/00 - 1/07$ and, $\overline{CS1}$ enables bits $1/08 - 1/015$.

\overline{CE} (Cache Chip Enable)

This active low signal, when active, enable writes to the data ram or reads from the data ram. It is a global signal, and controls both cache bank A and cache bank B. It's function is the same in both the set associative mode and the direct mapped mode. This input also functions as a chip enable controlled write.

\overline{OEA} , \overline{OEB} (Cache Output Enables)

In two-way mode, these active low signals enable cache bank A or B to drive the data bus. Either \overline{OEA} or \overline{OEB} is active during a read hit, depending on which bank is selected. Activation of \overline{OEA} simultaneous with \overline{OEB} will cause both banks to become deselected. In direct mode, these inputs will be externally wired together and A12 will determine which $4K \times 16$ memory bank is enabled.

\overline{WEA} , \overline{WEB} (Cache Write Enables)

In two-way mode, these active low signals enable cache bank A or B to receive data from the data bus. Either \overline{WEA} or \overline{WEB} is enabled in a read miss update or write hit. In direct mode, these inputs will be externally wired together and A12 will determine which $4K \times 16$ memory bank will be enabled for writing.

A0 – A11 (Addresses)

The address input provide the address into the SRAM array. These signals are latched on the trailing edge of CALEN.

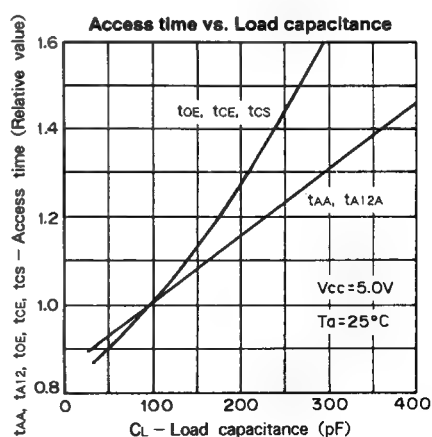
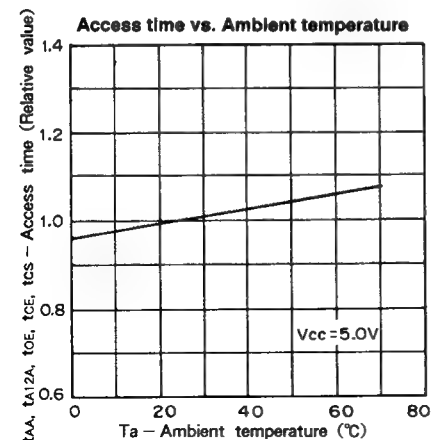
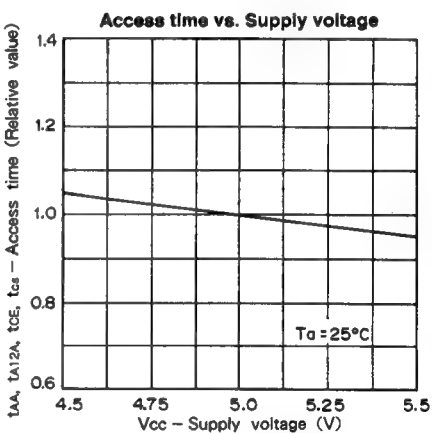
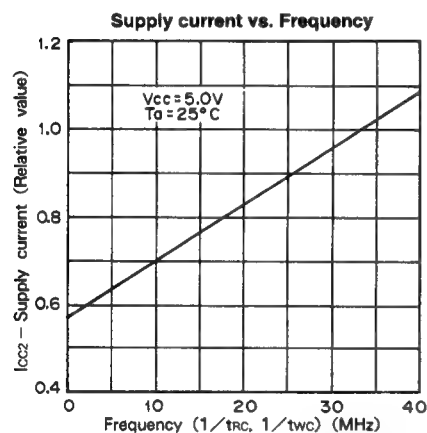
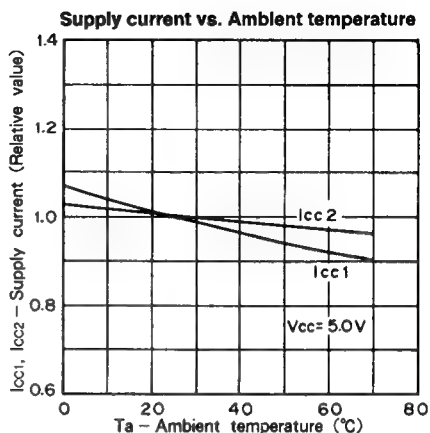
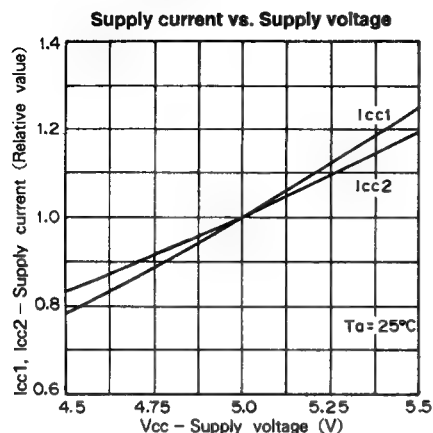
A12 (Address)

In two-way mode, the upper address input A12 will be a "don't care" and will be externally wired to ground.

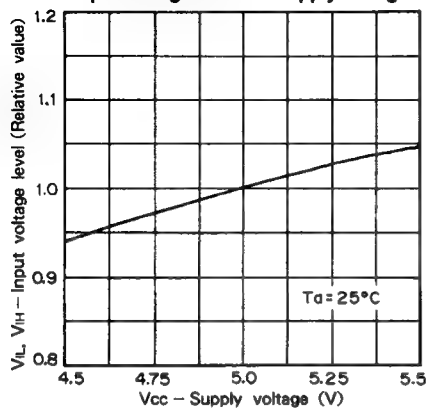
In direct mode, A12 will determine which $4K \times 16$ memory bank is enabled by \overline{WEA} and \overline{WEB} , and \overline{OEA} and \overline{OEB} .

Unlike the other address lines, A12 is not latched.

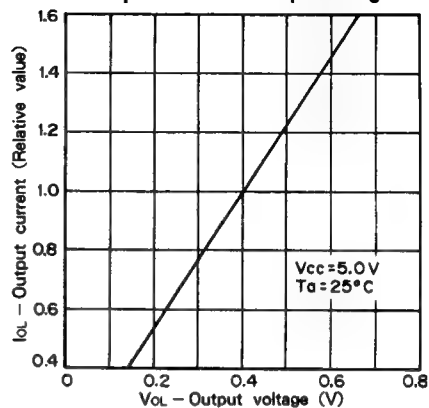
Example of Representative Characteristics



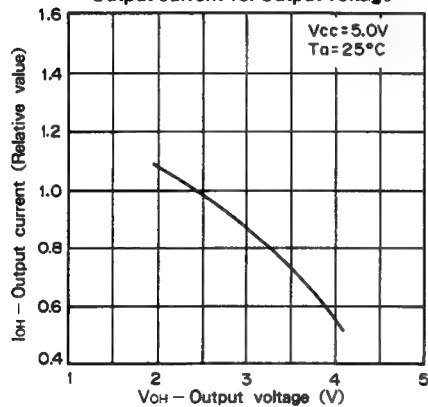
Input voltage level vs. Supply voltage



Output current vs. Output voltage

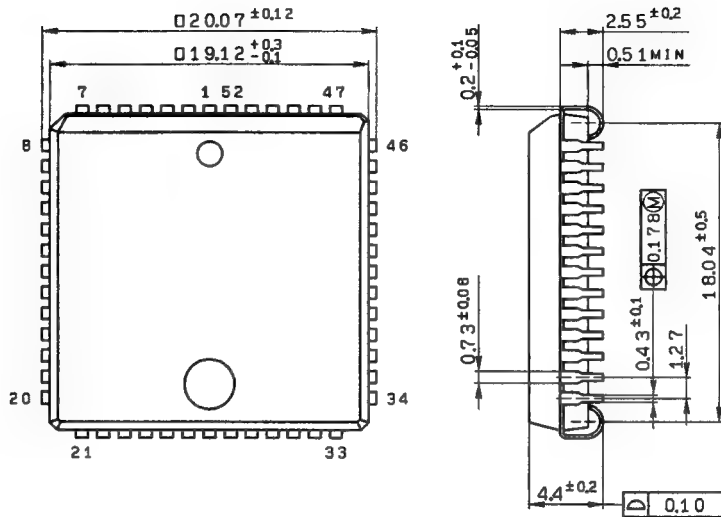


Output current vs. Output voltage



Package Outline Unit : mm

52 pin PLCC (Plastic)



SONY NAME	PLCC-52P-01
EIAJ NAME	*QFJ052-P-S750-A
JEDEC CODE	MO-047-AD

Description

The CXK77910J is a 1,179,648 bit Self-Timed Static Random Access Memory organized as 128K words by 9 bits. This STRAM integrates Input Registers, High Speed SRAM and Output Registers onto a single monolithic circuit. All Registers are triggered with the positive edge of an external clock (CLK). At the positive edge of CLK, the RAM data of the previous CLK cycle is presented. Write operation is initiated by the positive edge of CLK and internally self-timed. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Function

There are three possible user transactions with the STRAM. (Read operation, write operation and deselect operation.)

The read operation requires $\overline{WE} = \text{"HIGH"}$ and $\overline{OE} = \text{"low"}$ on the positive edge of CLK.

The memory location pointed to by the contents of the Address registers is read internally and the contents of the location are captured in the Data-out registers on the next positive edge of CLK. The state of Data-out will reflect the contents of the Data-out registers.

The write operation requires $\overline{CE} = \overline{WE} = \text{"LOW"}$ on the positive edge of CLK. The memory location pointed to by the contents of the Address registers is written with the contents of the Data-in registers. The write operation is entirely self-timed, eliminating critical timing edges.

The deselect cycle requires $\overline{CE} = \text{"HIGH"}$ or $\overline{OE} = \overline{WE} = \text{"HIGH"}$ on the positive edge of CLK. Write operation and internal read operation are disabled during the clock cycle. The data outputs are forced to a high impedance state during the next clock cycle. During the deselect cycle by $\overline{CE} = \text{"HIGH"}$, STRAM turns to power down mode.

The write cycle needs three preceding deselect cycles since the data for the write cycle must be supplied to I/O terminals during high impedance state. But immediately after power-on of the STRAM, the write operation can start on the first positive edge of CLK since the I/O terminals are initialized to be in high-impedance state.

32 pin SOJ (Plastic)



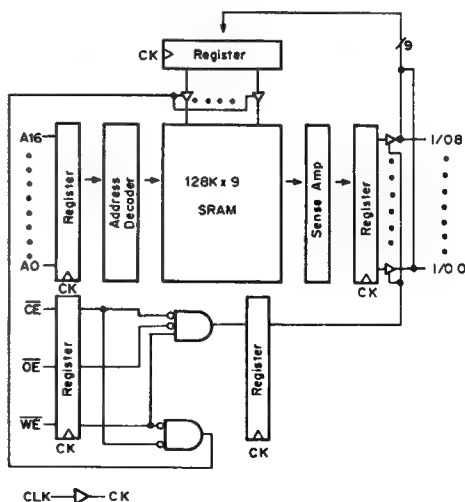
Features

- Fast Cycle Time: (Cycle) (Frequency)
CXK77910J-17 16.6ns 60MHz
CXK77910J-20 20.0ns 50MHz
- Fast Clock to Data Valid
CXK77910J-17/20 10ns
- Available in Plastic 32 pin 400mil SOJ
- All inputs and outputs registered with clock
- Direct TTL compatible
- Low power consumption (min. cycle, 100% duty)
CXK77910J-17/20 715mW (Max.)

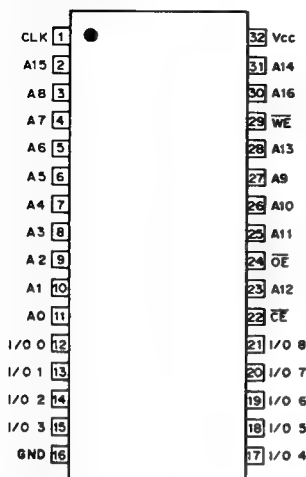
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description (1)

Symbol	Description
A ₀ to A ₁₆	Address input
I/O ₀ to I/O ₈	Data input/output
\overline{CE}	Chip enable input
\overline{OE}	Output enable input
\overline{WE}	Write enable input
CLK	Clock input
Vcc	+5V power supply
GND	Ground

Pin Description (2)

CLK (Clock, positive edge triggered)

All timing is controlled by the positive edge of CLK. All synchronous input and output signals are registered on the positive edge of CLK with set-up and hold times referenced to that edge.

Since only one edge of CLK is referenced, the duty cycle of CLK is not critical.

A₀ to A₁₆ (Address)

The Address inputs are decoded on-chip to select one of 131,072 words.

The state of the Address inputs is registered into the Address register on the positive edge of CLK.

The Address inputs must be valid during every positive edge with all set-up and hold times referenced to that edge.

I/O₀ to I/O₈ (I/O Common)

I/O terminals are three-state and data-input/data-output common.

The state is defined by the Control block. The data inputs for write operation must be valid during every positive edge of CLK with all set-up and hold times referenced to that edge. The data outputs are triggered by the edge of CLK and the contents in Output-Registers are presented.

\overline{WE} (Synchronous Write Enable, active low)

The \overline{WE} is used to indicate whether a read or write operation is to be performed. If the STRAM is selected, \overline{WE} is LOW to perform a write operation. The \overline{WE} is registered on every positive edge of CLK with set-up and hold times referenced to that edge. The internal timing required to store data into the memory array is self-timed.

\overline{OE} (Synchronous Output Enable, active low)

The \overline{OE} is used to indicate that a read operation is to be performed. If the STRAM is selected, the \overline{OE} is LOW to perform a read operation. The \overline{OE} is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

\overline{CE} (Synchronous Chip Enable, active low)

The \overline{CE} is used to select the STRAM when LOW (or deselect when HIGH). When selected, the STRAM will perform a read or write operation. The state of the \overline{CE} is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 to V _{CC} +0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL}=-1V Min. for 3ns per cycle.**Electrical Characteristics****• DC and operating characteristics** (V_{CC}=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input leakage current	I _I	V _{IN} =GND to V _{CC}	-1	1	μA
Output leakage current	I _{LO}	V _{I/O} =GND to V _{CC} , CE=V _{IH} or OE=V _{IH} or WE=V _{IL}	-1	1	μA
Operating power supply current	I _{CC1}	CE=V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	—	100	mA
Average operating current	I _{CC2}	Cycle=Min, Duty=100%, I _{OUT} =0mA	—	130	mA
Standby current	I _{SB1}	CE ≥ V _{CC} -0.2V V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	—	1	mA
	I _{SB2}	CE=V _{IH} , I _{OUT} =0mA Cycle=Min, Duty=100%	—	80	mA
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} =4.0mA	—	0.4	V

Truth tables

CLK	CE	OE	WE	Operation
$\overline{\text{L}}$	H	x	x	Outputs High-Z, Write Disabled, Power Down
$\overline{\text{L}}$	x	H	H	Outputs High-Z, Write Disabled
$\overline{\text{L}}$	L	L	H	Read I/O 0 to 8
$\overline{\text{L}}$	L	x	L	Write I/O 0 to 8

x : "H" or "L"

I/O capacitance

(Ta=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	5	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

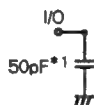
AC characteristics

• AC test conditions

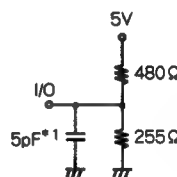
(V_{CC}=5V ± 10%, Ta=0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} =3.0V
Input pulse low level	V _{IL} =0V
Input rise time	t _r =3ns
Input fall time	t _f =3ns
Input and output reference level	1.5V
Output load (See test circuit below)	Fig. 1

Output Load (1)



Output Load (2) *2



*1 including scope and jig capacitance

*2 for t_{CKH02}, t_{CKH02}

Fig. 1

• Read cycle

Item	Symbol	-17		-20		Unit
		Min	Max	Min	Max	
Read cycle time	tCKHCKH	16.6	—	20	—	ns
Clock high pulse width	tCKHCKL	5	—	5	—	ns
Clock low pulse width	tCKLCKH	5	—	5	—	ns
Clock to data valid	tCKHCV	—	10	—	10	ns
Address setup to clock high	tAVCKH	3	—	3	—	ns
Address hold from clock high	tCKHAX	0.5	—	1	—	ns
Chip enable setup to clock high	tCEVCKH	3	—	3	—	ns
Chip enable hold from clock high	tCKHCEX	0.5	—	1	—	ns
Output enable setup to clock high	tOEVCKH	3	—	3	—	ns
Output enable hold from clock high	tCKHOEX	0.5	—	1	—	ns
Output hold from clock high	tCKHQX1	2	—	3	—	ns
Clock high to output low-Z	tCKHQX2 *	0	—	0	—	ns
Clock high to output high-Z	tCKHQZ *	—	8	—	10	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

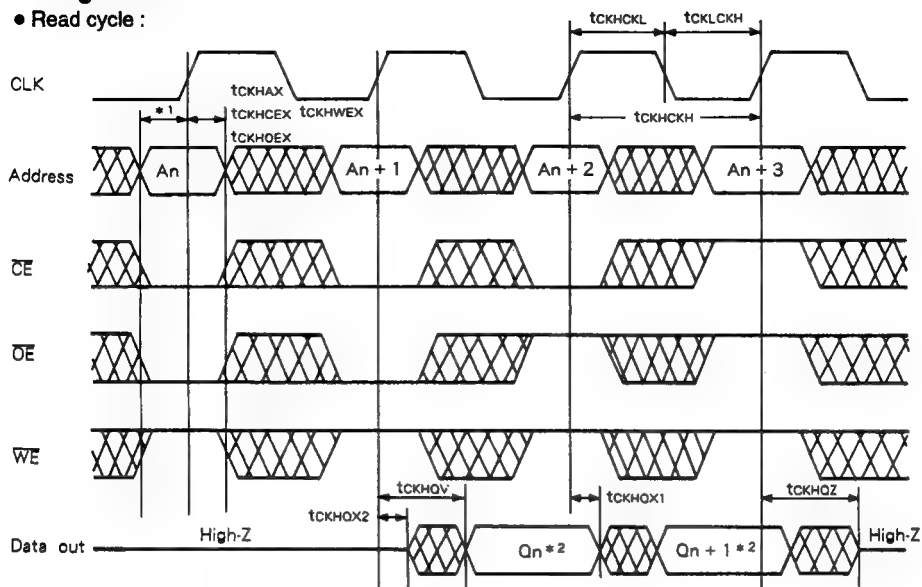
This parameter is sampled and is not 100% tested.

• Write cycle

Item	Symbol	-17		-20		Unit
		Min	Max	Min	Max	
Write cycle time	tCKHCKH	16.6	—	20	—	ns
Clock high pulse width	tCKHCKL	5	—	5	—	ns
Clock low pulse width	tCKLCKH	5	—	5	—	ns
Address setup to clock high	tAVCKH	3	—	3	—	ns
Address hold from clock high	tCKHAX	0.5	—	1	—	ns
Chip enable setup to clock high	tCEVCKH	3	—	3	—	ns
Chip enable hold from clock high	tCKHCEX	0.5	—	1	—	ns
Write enable setup to clock high	tWEVCKH	3	—	3	—	ns
Write enable hold from clock high	tCKHWEX	0.5	—	1	—	ns
Input data setup to clock high	tDVCKH	3	—	3	—	ns
Input data hold from clock high	tCKHDX	0.5	—	1	—	ns

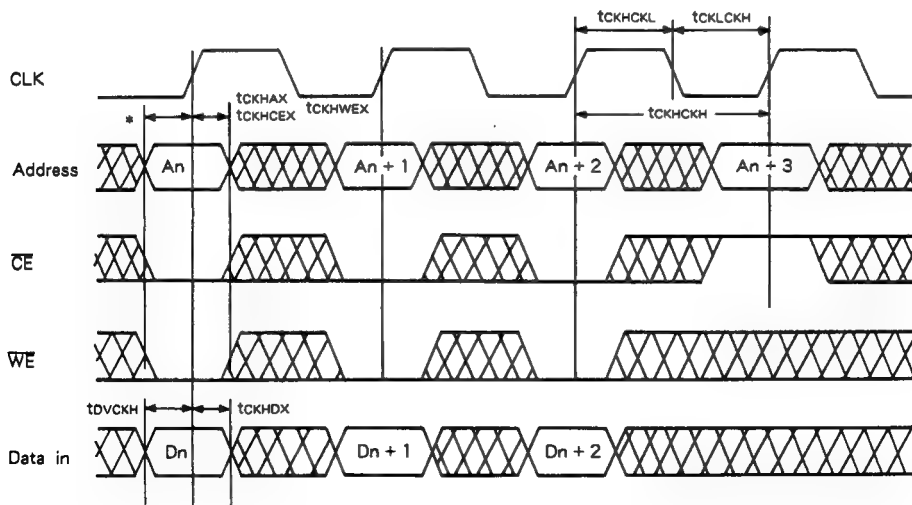
Timing Waveform

• Read cycle :



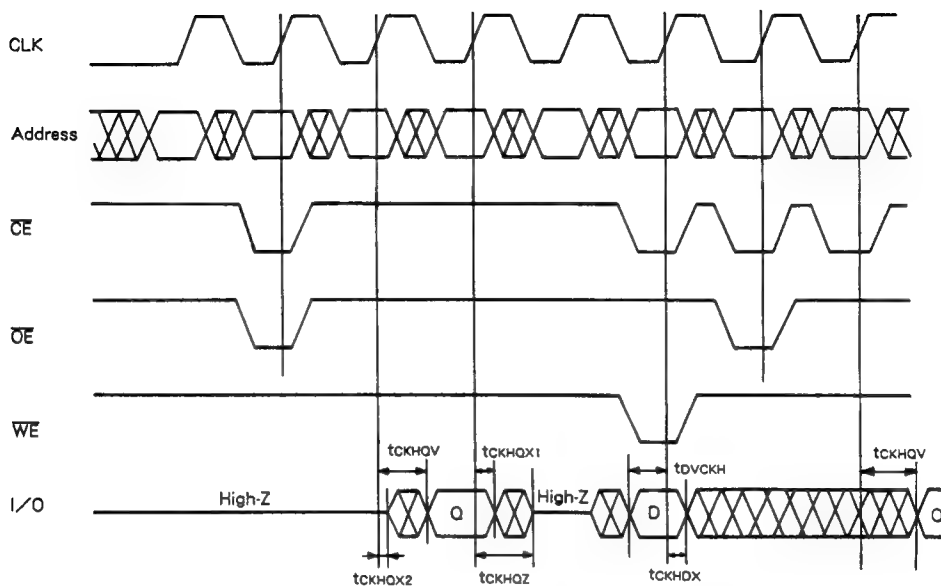
* 1 tAVCKH, tCEVCKH, tOEVCKH, tWEVCKH

* 2 Valid data from CLK high is the data from the previous cycle.

• Write cycle: $\overline{OE}=V_{IH}$ or V_{IL} 

* tAVCKH, tCEVCKH, tWEVCKH

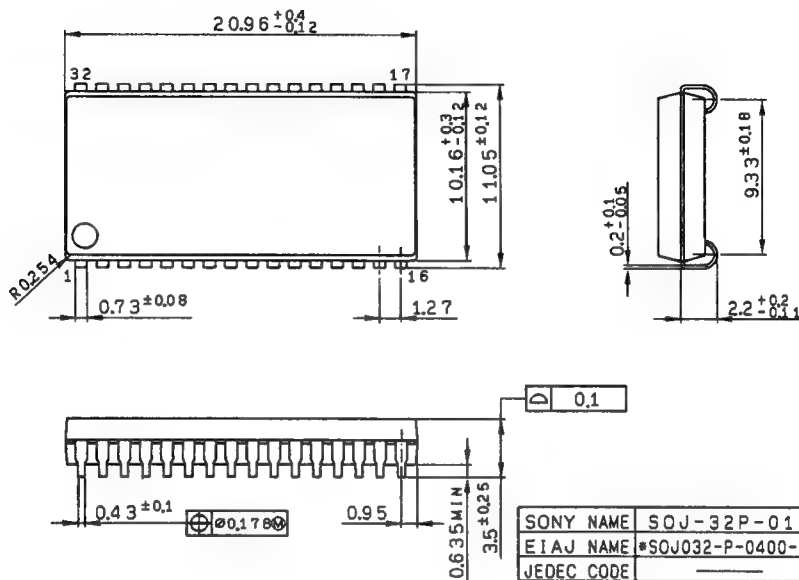
• Alternate Read/Write cycle

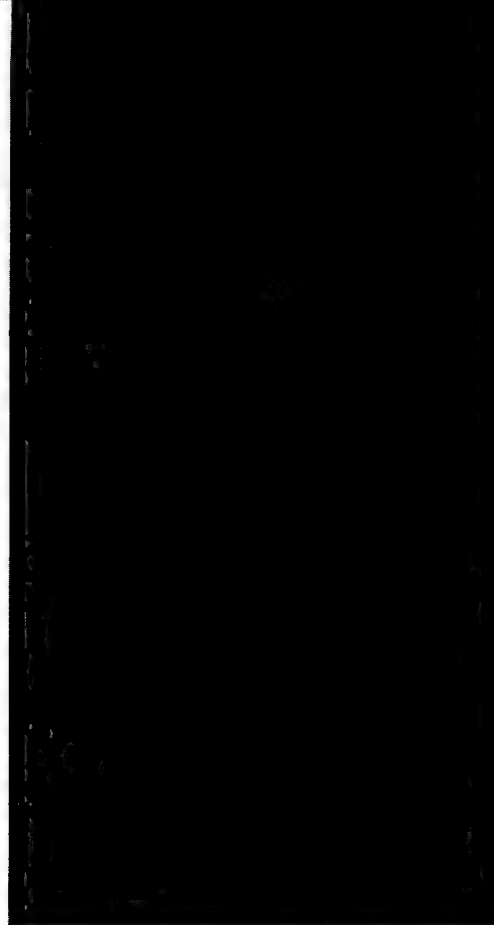


Package Outline

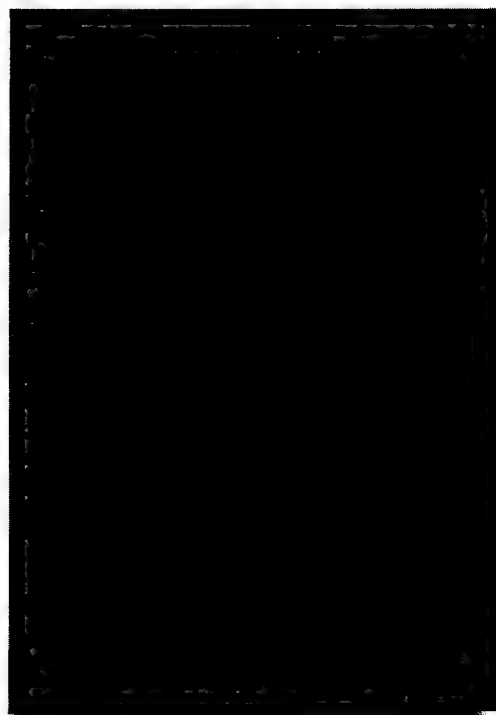
Unit : mm

32pin SOJ (Plastic) 400mil 1.3g





Mask ROM



3) Mask ROM

Type	Memorie capacity	Functions	Access time	Page
CXK384000	4M bit	256k × 16/512k × 8bit	200ns	377
CXK384001	4M bit	512k × 8bit	200ns	384
CXK388000	8M bit	512k × 16bit/1024k × 8bit	200ns	391

SONY**CXK384000****4,194,304-bit CMOS Mask Programmable ROM****Description**

The CXK384000 is a 4,194,304-bit CMOS silicon gate mask programmable read only memory. This chip is organized as 524,288 words by 8-bit output for the byte mode and 262,144 words by 16-bit output for the word mode. Selection of either mode is possible.

Features

- Access time (Max.)
 - Address access time 200ns
 - Chip enable access time 200ns
 - Output enable access time 70ns
- Word organization
 - 524,288 words × 8-bit (Byte mode)
 - 262,144 words × 16-bit (Word mode)
- Power consumption (Typ.)
 - 100mW (Operation)
 - 0.5mW (Standby, TTL input level)
 - 5nW (Standby, CMOS input level)
- Static operation
- I/O TTL compatible
- 3 state output
- Single 5V power supply operation

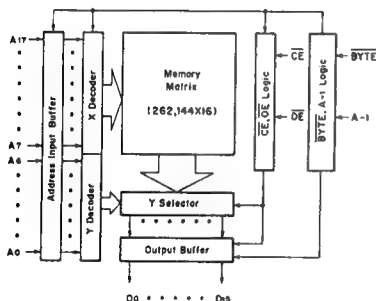
40 pin DIP (Plastic)

**Function**

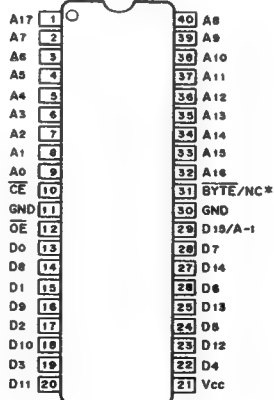
4,194,304-bit mask programmable ROM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration**

(Top View)

**Pin Description**

Symbol	Description
A-1 to A-17	Address input
D0 to D15	Data output
BYTE	Selection of 8/16-bit
CE	Chip enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground

* Pin 31 function can be programmed to one of the following by means of the mask option

- 1) BYTE : Selection of 8 or 16-bit possible
- 2) NC : Fixed to 16 bit output mode

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 * to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Output voltage	V _{OUT}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature * time	T _{solder}	260 * 10	°C * sec

* V_{CC}, V_{IN}, V_{OUT}=-3.5V Min. for pulse width less than 20ns.**Truth Table**

\overline{CE}	\overline{OE}	BYTE	A-1	Mode	D ₀ to D ₇	D ₈ to D ₁₄	D ₁₅	V _{CC} current
H	X	X	X	Not selected	High Z	High Z	High Z	I _{SB1} , I _{SB2}
L	H	X	X	Not selected	High Z	High Z	High Z	I _{CC1} , I _{CC2}
L	L	H	X	Selected	D ₀ to D ₇	D ₈ to D ₁₄	D ₁₅	I _{CC1} , I _{CC2}
L	L	L	L	Selected	D ₀ to D ₇	High Z	A-1	I _{CC1} , I _{CC2}
L	L	L	H	Selected	D ₈ to D ₁₅	High Z	A-1	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ. *	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 **	—	0.8	V

* V_{CC}=5V, Ta=25°C** V_{IL}=-3.0V Min. for pulse width less than 20ns**Electrical Characteristics****• DC characteristics**(V_{CC}=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Conditions	Min.	Typ. *	Max.	Unit
Input leakage current	I _I	0V ≤ V _{IN} ≤ V _{CC}	-1	—	1	μA
Output leakage current	I _O	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ 0V ≤ V _{OUT} ≤ V _{CC}	-1	—	1	μA
Operating current (DC)	I _{CC1}	$\overline{CE}=V_{IL}$, I _{OUT} =0mA	—	10	40	mA
Average operating current	I _{CC2}	$\overline{CE}=V_{IL}$, I _{OUT} =0mA Duty=100%, Cycle=Min.	—	20	50	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$	—	0.001	30	μA
	I _{SB2}	$\overline{CE}=V_{IH}$	—	0.1	2.0	mA
Output high voltage	V _{OH}	I _{OH} =-400 μA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	V

* V_{CC}=5V, Ta=25°C

I/O Capacitance

(Ta=25°C, f=1MHz)

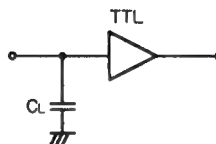
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	8	15	pF
Output capacitance	C _{OUT}	V _{OUT} =0V	—	6	15	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

● AC test conditions (V_{CC}=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} =2.4V
Input pulse low level	V _{IL} =0.6V
Input rise time	t _r =10ns
Input fall time	t _f =10ns
Input timing reference level	V _{IL} =1.5V, V _{IH} =1.5V
Output timing reference level	V _{OL} =1.5V, V _{OH} =1.5V
Output load conditions	C _L =100pF*, 1TTL

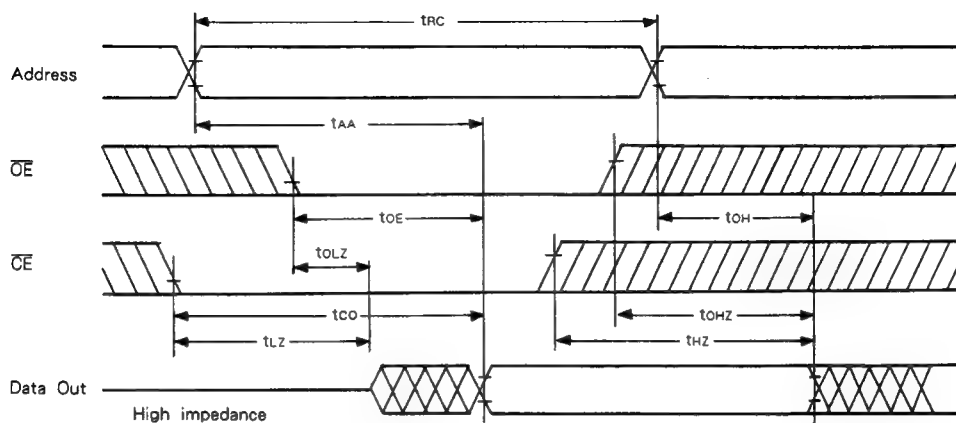
* C_L includes scope and jig capacitances.

● AC characteristics

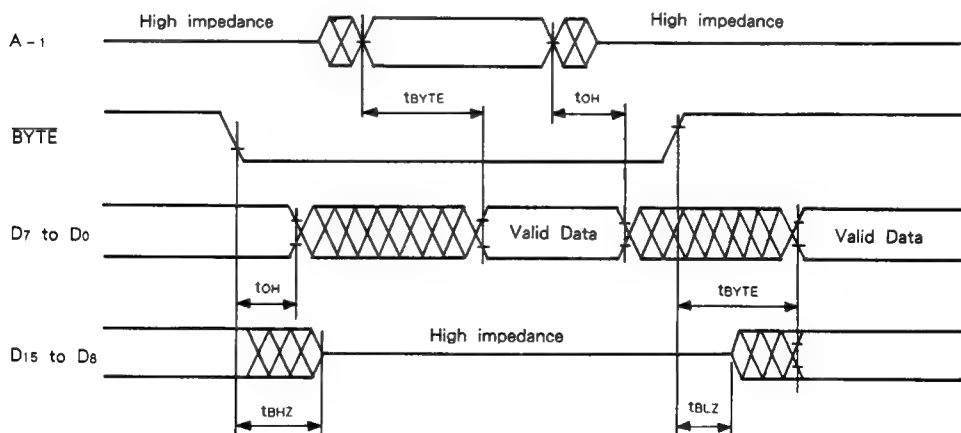
Item	Symbol	Min.	Typ.	Max.	Unit
Read cycle time	t _{RC}	200	—	—	ns
Address access time	t _{AA}	—	—	200	ns
Chip enable access time	t _{CO}	—	—	200	ns
Output enable access time	t _{OE}	—	—	70	ns
BYTE access time	t _{BYTE}	—	—	200	ns
Output data hold time	t _{OH}	0	—	—	ns
Output enable time (from \overline{CE})	t _{LZ}	0	—	—	ns
Output enable time (from \overline{OE})	t _{OLZ}	0	—	—	ns
Output enable time (from \overline{BYTE})	t _{BLZ}	0	—	—	ns
Output disable time (from \overline{CE})	t _{HZ}	—	40	70	ns
Output disable time (from \overline{OE})	t _{OHZ}	—	40	70	ns
Output disable time (from \overline{BYTE})	t _{BHZ}	—	40	70	ns

Timing Waveform

- Read cycle (1) : BYTE="V_{IH}" or "V_{IL}" is fixed

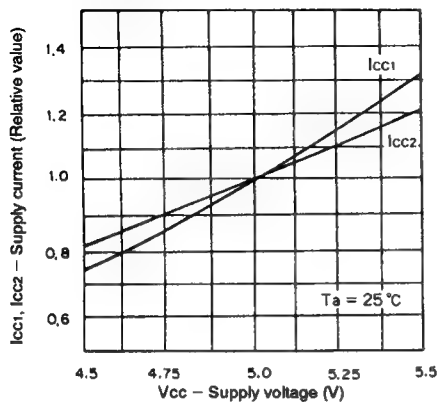


- Read cycle (2) : Selection of word mode or byte mode

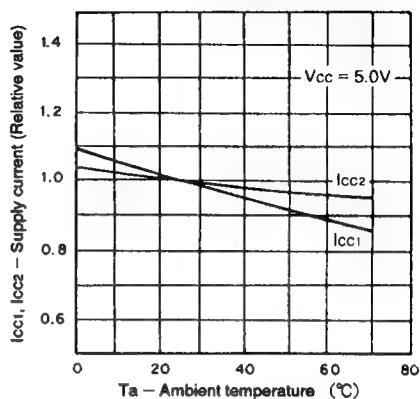


Example of Representative Characteristics

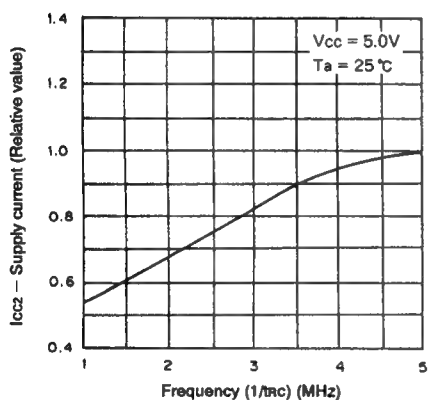
Supply current vs. Supply voltage



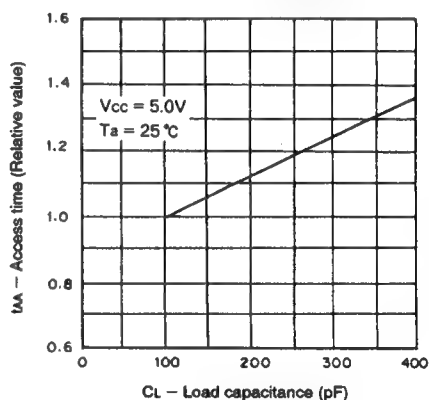
Supply current vs. Ambient temperature



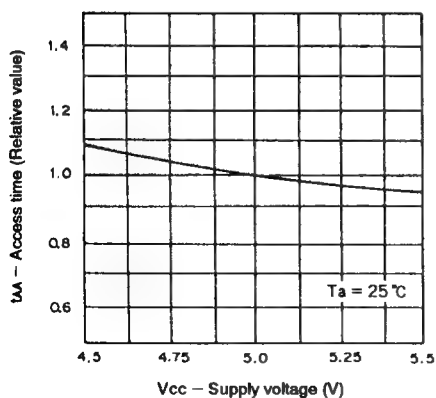
Supply current vs. Frequency



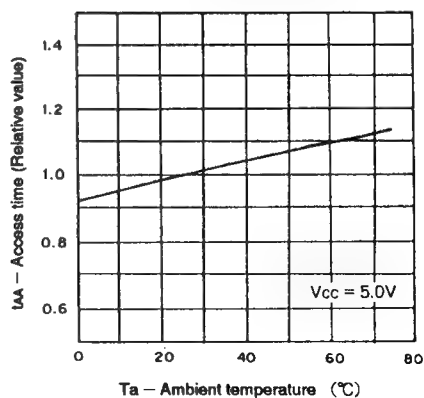
Access time vs. Load capacitance



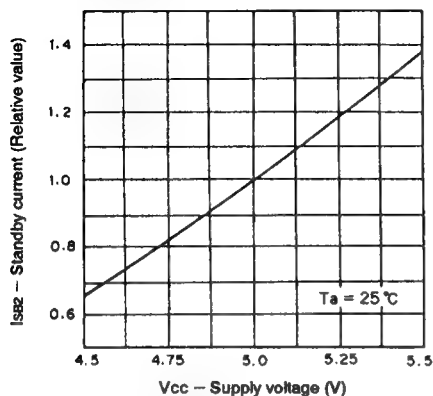
Access time vs. Supply voltage



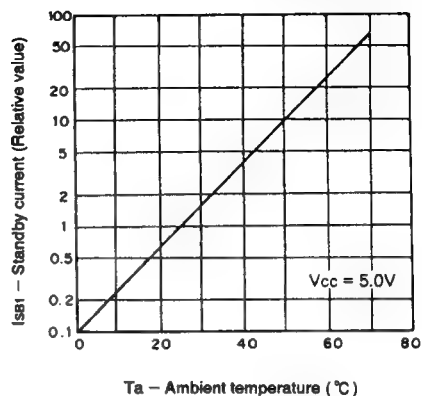
Access time vs. Ambient temperature



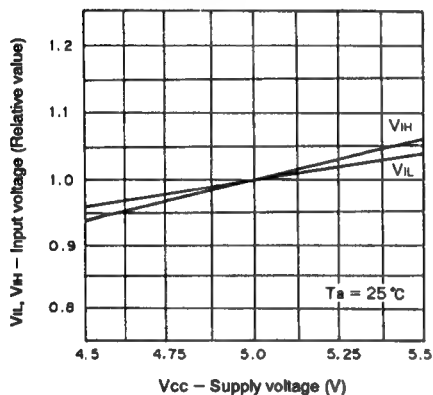
Standby current vs. Supply voltage



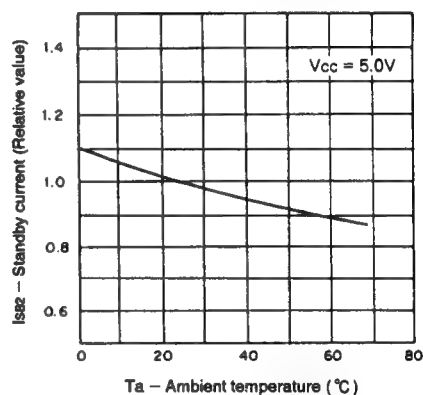
Standby current vs. Ambient temperature



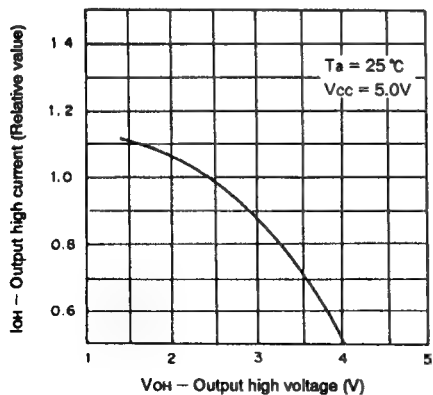
Input voltage level vs. Supply voltage



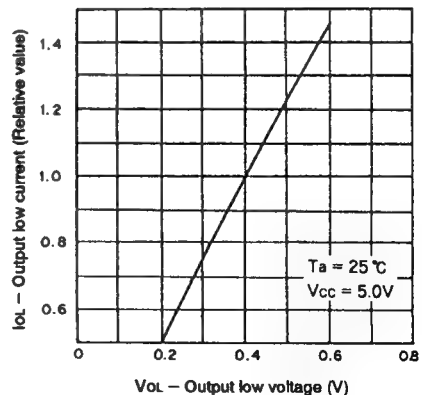
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



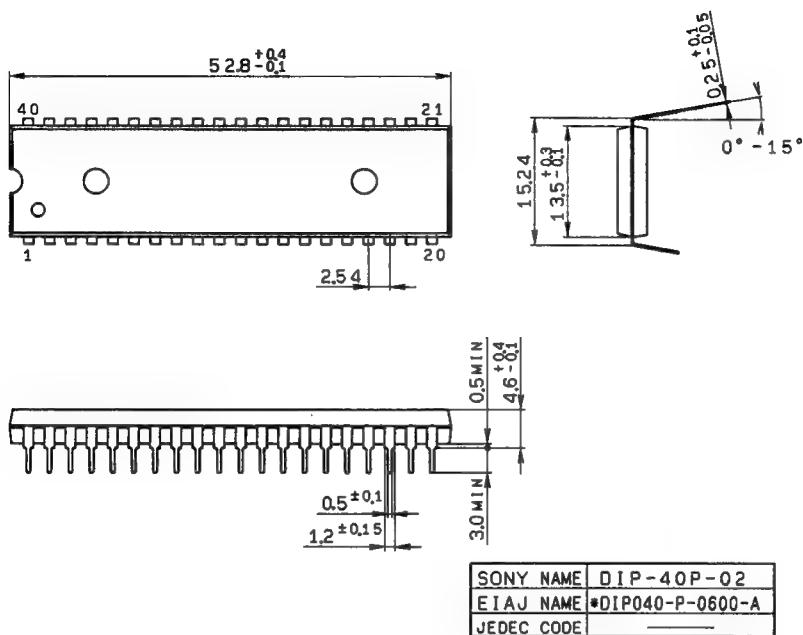
Output low current vs. Output low voltage



Package Outline

Unit : mm

40pin DIP (Plastic) 600mil



524,288-word × 8-bit CMOS Mask Programmable ROM

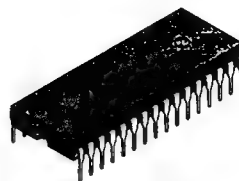
Description

CXK384001 is a CMOS mask-programmable ROM organized as 524,288 words by 8-bit. The chip enable input disable outputs and sets the chip to low power standby mode.

Features

- Access time (Max.)
 - Address access time 200ns
 - Chip enable access time 200ns
 - Output enable access time 70ns
- Power consumption (Typ.)
 - 100mW (Operation)
 - 0.5mW (Standby TTL input level)
 - 5.0nW (Standby CMOS input level)
- Static operation
- I/O TTL compatible
- Tri-state output
- Single +5V power supply operation

32 pin DIP (Plastic)



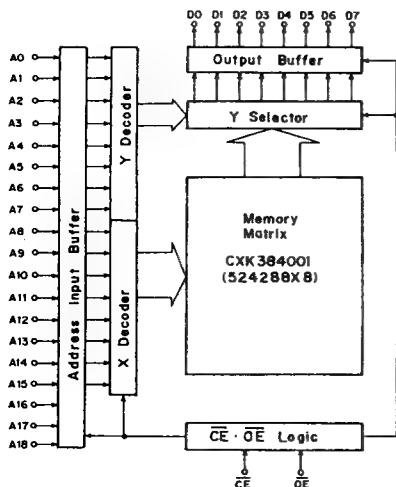
Functions

524,288-word × 8-bit mask programmable ROM

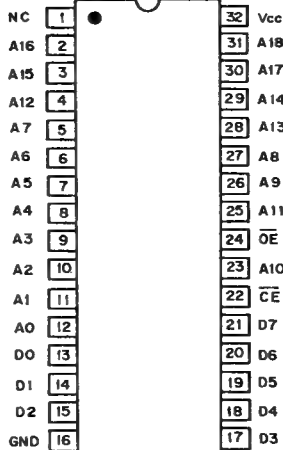
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A18	Address input
D0 to D7	Data output
\overline{CE}	Chip enable input
\overline{OE}	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25 °C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Output voltage	V _{OUT}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

Note) * V_{IN}, V_{OUT} = - 3.5V Min. for pulse width less than 20ns.**Truth Table**

\overline{CE}	\overline{OE}	Mode	Output pin	V _{CC} current
H	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	L	Selected	Data output	I _{CC1} , I _{CC2}

Note) X : "H" or "L"**DC Recommended Operating Conditions** (Ta = 0 to + 70 °C, GND = 0V)

Item	Symbol	Min.	Typ.*	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3**	—	0.8	V

Note) * V_{CC} = 5V, Ta = 25 °C** V_{IL} = - 3.0V Min. for pulse width less than 20ns.**Electrical Characteristics****DC characteristics**(V_{CC} = 5V ± 10 %, GND = 0V, Ta = 0 to + 70 °C)

Item	Symbol	Test Condition	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	0V ≤ V _{IN} ≤ V _{CC}	- 1	—	1	μA
Output leakage current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ 0V ≤ V _{OUT} ≤ V _{CC}	- 1	—	1	μA
Operating current (DC)	I _{CC1}	$\overline{CE} = V_{IL}$, I _{OUT} = 0mA	—	10	40	mA
Average operating current	I _{CC2}	$\overline{CE} = V_{IL}$, I _{OUT} = 0mA Duty = 100 %, Minimum cycle	—	20	50	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	—	0.001	30	μA
	I _{SB2}	$\overline{CE} = V_{IH}$	—	0.1	2.0	mA
Output high voltage	V _{OH}	I _{OH} = - 400 μA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	V

Note) * V_{CC} = 5V, Ta = 25 °C

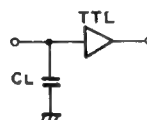
Capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	8	15	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V	—	6	15	pF

Note) This parameter is sampled and is not 100% tested.**AC characteristics****AC test condition** (V_{CC} = 5V ± 10%, Ta = 0 to +70°C)

Item	Condition
Input pulse high level	V _{IH} = 2.4V
Input pulse low level	V _{IL} = 0.6V
Input rise time	t _r = 10ns
Input fall time	t _f = 10ns
Input timing reference level	V _{IL} = V _{IH} = 1.5V
Output timing reference level	V _{OL} = V _{OH} = 1.5V
Output load	C _L * = 100pF, 1TTL

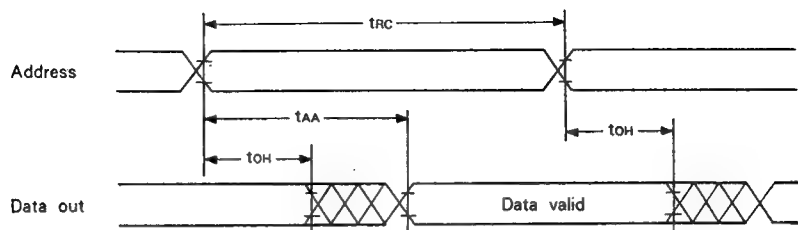
• Test circuit**Note)** C_L includes scope and jig capacitances.**AC characteristics**

Item	Symbol	Min.	Typ.**	Max.	Unit
Read cycle time	t _{RC}	200	130	—	ns
Address access time	t _{AA}	—	120	200	ns
Chip enable access time	t _{CO}	—	130	200	ns
Output enable access time	t _{OE}	—	40	70	ns
Output data hold time	t _{OH}	0	—	—	ns
Output enable time (from \overline{CE})	t _{LZ}	0	—	—	ns
Output enable time (from \overline{OE})	t _{OLZ}	0	—	—	ns
Output disable time (from \overline{CE})	t _{HZ} *	—	40	70	ns
Output disable time (from \overline{OE})	t _{OHZ} *	—	40	70	ns

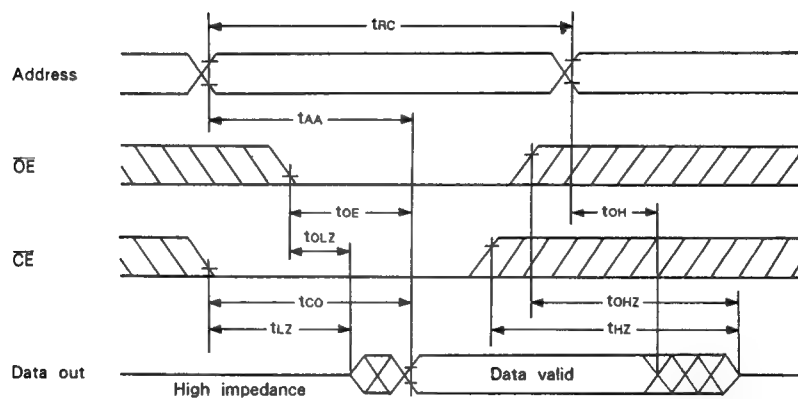
Note) * t_{HZ} and t_{OHZ} are defined as the time required for the outputs to turn to high impedance state and are not referred to as output voltage levels.** V_{CC} = 5V, Ta = 25°C

Timing Waveform

- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$

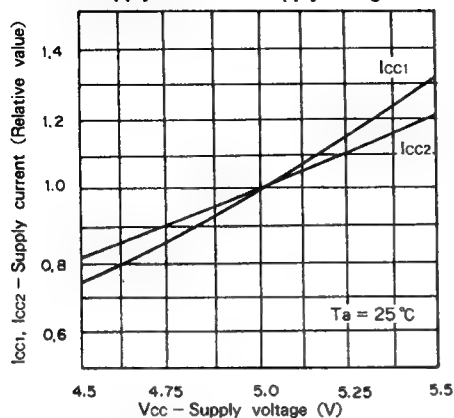


- Read cycle (2)

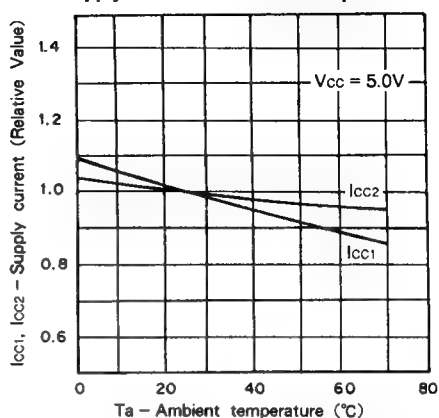


Example of Representative Characteristics

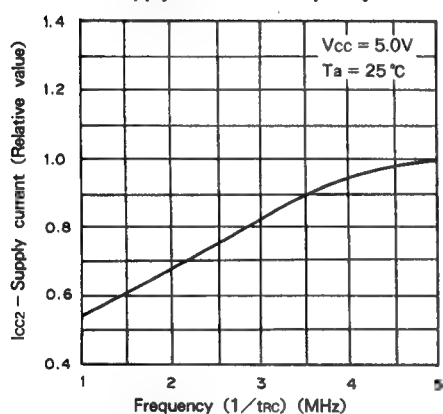
Supply current vs. Supply voltage



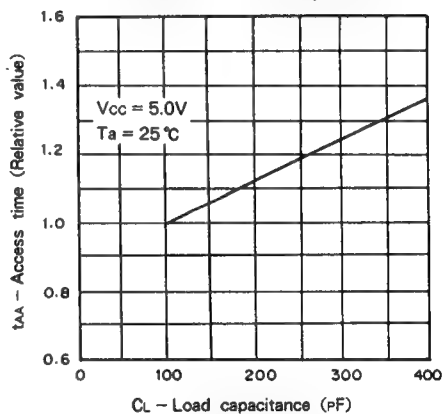
Supply current vs. Ambient temperature



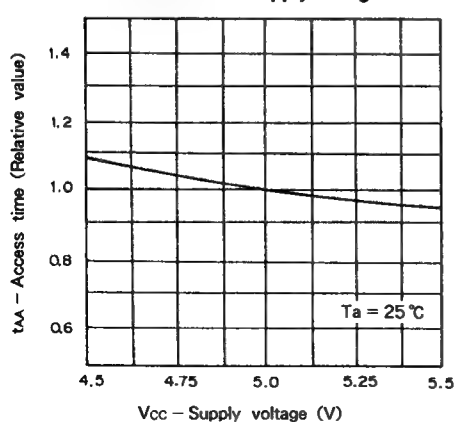
Supply current vs. Frequency



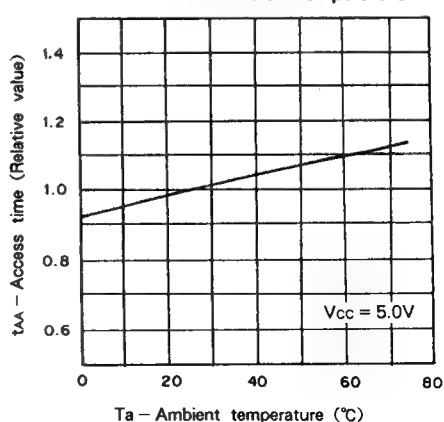
Access time vs. Load capacitance



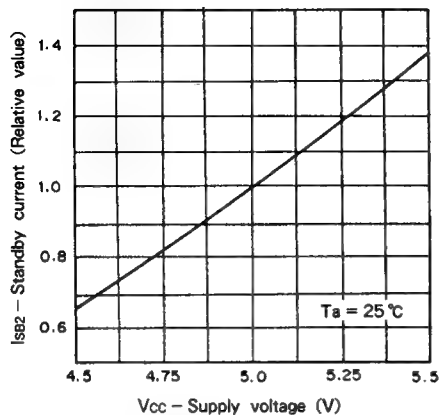
Access time vs. Supply voltage



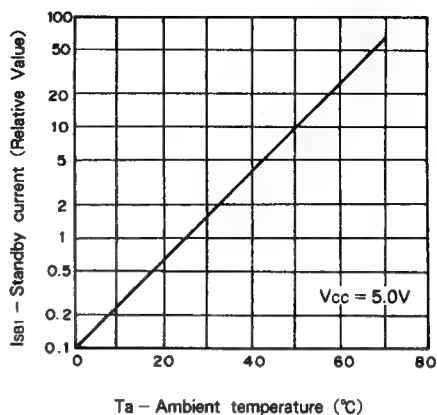
Access time vs. Ambient temperature



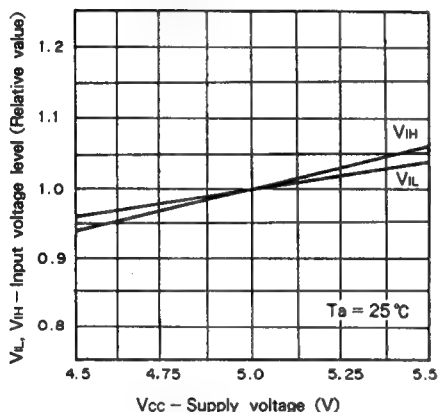
Standby current vs. Supply voltage



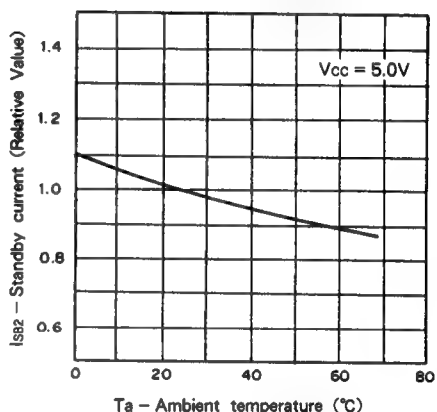
Standby current vs. Ambient temperature



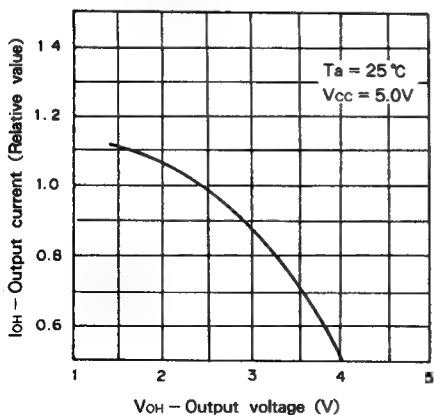
Input voltage level vs. Supply voltage



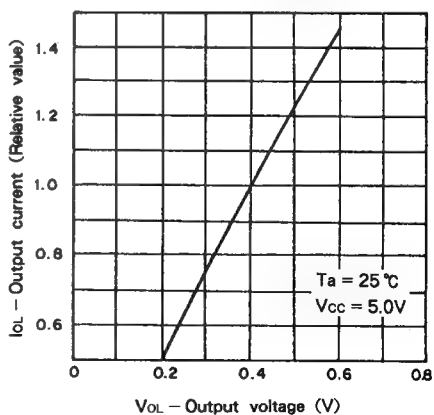
Standby current vs. Ambient temperature



Output current vs. Output voltage

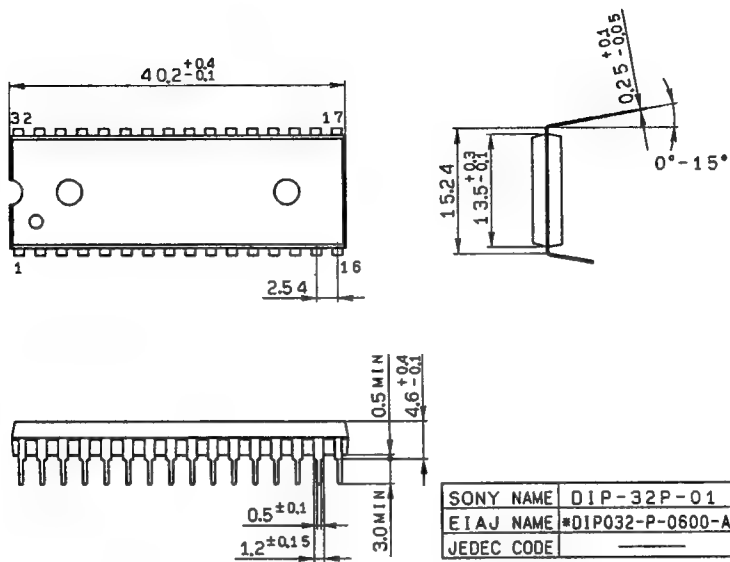


Output current vs. Output voltage



Package Outline Unit : mm

32 pin DIP (Plastic) 600mil 4.5g



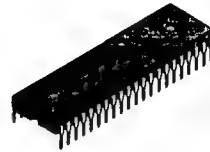
SONY**CXK388000****8,388,608-bit CMOS Mask Programmable ROM****Description**

The CXK388000 is a 8,388,608-bit CMOS silicon gate mask programmable read only memory. This chip is organized as 1,048,576 words by 8-bit output for the byte mode and 524,288 words by 16-bit output for the word mode. Selection of either mode is possible.

Features

- Access time (Max.)
 - Address access time 200ns
 - Chip enable access time 200ns
 - Output enable access time 70ns
- Word organization
 - 1,048,576 words × 8-bit (Byte mode)
 - 524,288 words × 16-bit (Word mode)
- Power consumption (Typ.)
 - 100mW (Operation)
 - 0.5mW (Standby, TTL input level)
 - 5nW (Standby, CMOS input level)
- Static operation
- I/O TTL compatible
- 3 state output
- Single 5V power supply operation

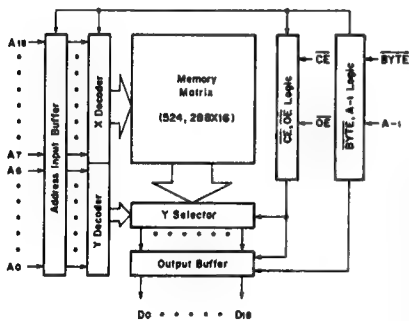
42 pin DIP (Plastic)

**Function**

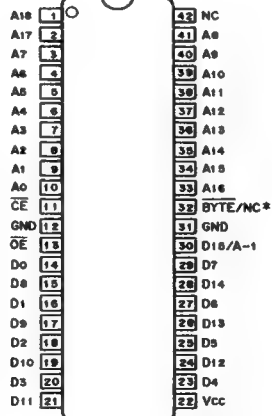
8,388,608-bit mask programmable ROM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration**

(Top View)

**Pin Description**

Symbol	Description
A-1 to A-18	Address input
D0 to D15	Data output
BYTE	Selection of 8/16-bit
CE	Chip enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground

* Pin 32 function can be programmed to one of the following by means of the mask option

- 1) BYTE : Selection of 8 or 16-bit possible
- 2) NC : Fixed to 16-bit output mode

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 * to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Output voltage	V _{OUT}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature * time	T _{solder}	260 * 10	°C * sec

* V_{CC}, V_{IN}, V_{OUT}=-3.5V Min. for pulse width less than 20ns.

Truth Table

CE	OE	BYTE	A-1	Mode	D ₀ to D ₇	D ₈ to D ₁₄	D ₁₅	V _{CC} current
H	X	X	X	Not selected	High Z	High Z	High Z	I _{SB1} , I _{SB2}
L	H	X	X	Not selected	High Z	High Z	High Z	I _{CC1} , I _{CC2}
L	L	H	X	Selected	D ₀ to D ₇	D ₈ to D ₁₄	D ₁₅	I _{CC1} , I _{CC2}
L	L	L	L	Selected	D ₀ to D ₇	High Z	A-1	I _{CC1} , I _{CC2}
L	L	L	H	Selected	D ₈ to D ₁₅	High Z	A-1	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ. *	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 **	—	0.8	V

* V_{CC}=5V, Ta=25°C** V_{IL}=-3.0V Min. for pulse width less than 20ns

Electrical Characteristics

• DC characteristics

(V_{CC}=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Conditions	Min.	Typ. *	Max.	Unit
Input leakage current	I _{LI}	0V ≤ V _{IN} ≤ V _{CC}	-1	—	1	μA
Output leakage current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ 0V ≤ V _{OUT} ≤ V _{CC}	-1	—	1	μA
Operating current (DC)	I _{CC1}	$\overline{CE}=V_{IL}$, I _{OUT} =0mA	—	10	40	mA
Average operating current	I _{CC2}	$\overline{CE}=V_{IL}$, I _{OUT} =0mA Duty=100%, Cycle=Min.	—	20	50	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$	—	0.001	30	μA
	I _{SB2}	$\overline{CE}=V_{IH}$	—	0.1	2.0	mA
Output high voltage	V _{OH}	I _{OH} =-400 μA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	V

* V_{CC}=5V, Ta=25°C

I/O Capacitance

(Ta=25°C, f=1MHz)

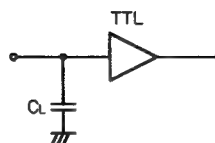
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	8	15	pF
Output capacitance	C _{OUT}	V _{OUT} =0V	—	6	15	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• **AC test conditions** (V_{CC}=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} =2.4V
Input pulse low level	V _{IL} =0.6V
Input rise time	t _r =10ns
Input fall time	t _f =10ns
Input timing reference level	V _{IL} =1.5V, V _{IH} =1.5V
Output timing reference level	V _{OL} =1.5V, V _{OH} =1.5V
Output load conditions	C _L =100pF*, 1TTL



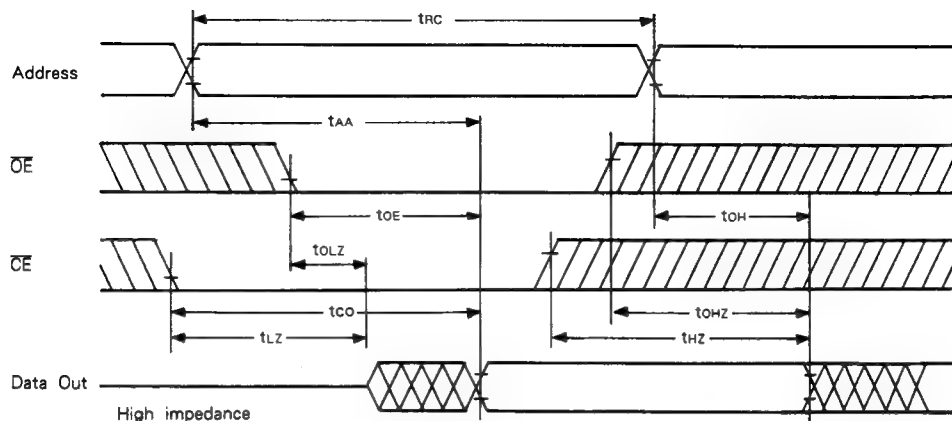
* C_L includes scope and jig capacitances.

• AC characteristics

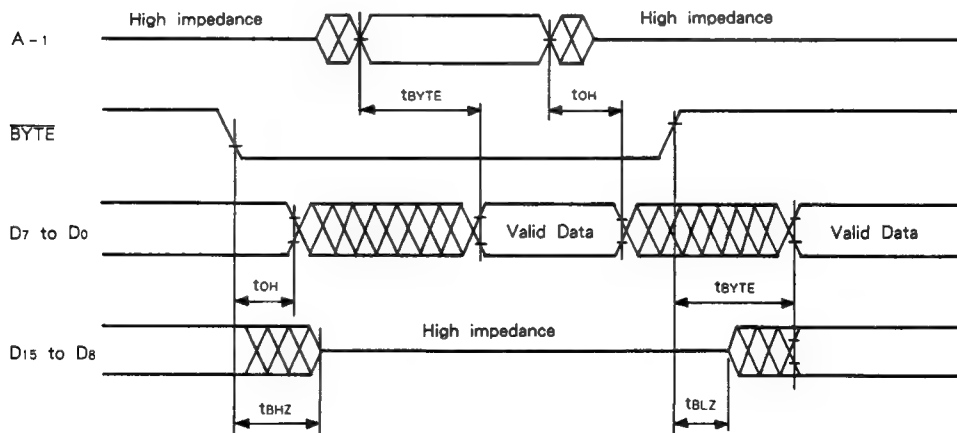
Item	Symbol	Min.	Typ.	Max.	Unit
Read cycle time	t _{RC}	200	—	—	ns
Address access time	t _{AA}	—	—	200	ns
Chip enable access time	t _{CO}	—	—	200	ns
Output enable access time	t _{OE}	—	—	70	ns
BYTE access time	t _{BYTE}	—	—	200	ns
Output data hold time	t _{OH}	0	—	—	ns
Output enable time (from \overline{CE})	t _{LZ}	0	—	—	ns
Output enable time (from \overline{OE})	t _{OLZ}	0	—	—	ns
Output enable time (from BYTE)	t _{BLZ}	0	—	—	ns
Output disable time (from \overline{CE})	t _{HZ}	—	40	70	ns
Output disable time (from \overline{OE})	t _{OHZ}	—	40	70	ns
Output disable time (from BYTE)	t _{BHZ}	—	40	70	ns

Timing Waveform

- Read cycle (1) : BYTE = "V_{IH}" or "V_{IL}" is fixed

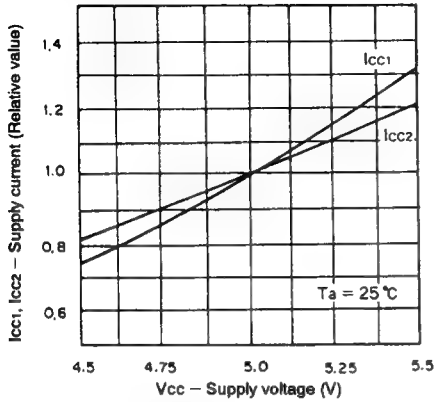


- Read cycle (2) : Selection of word mode or byte mode

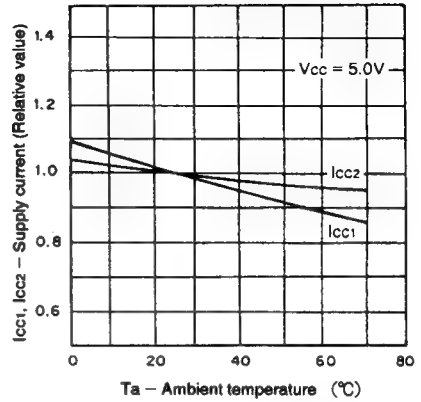


Example of Representative Characteristics

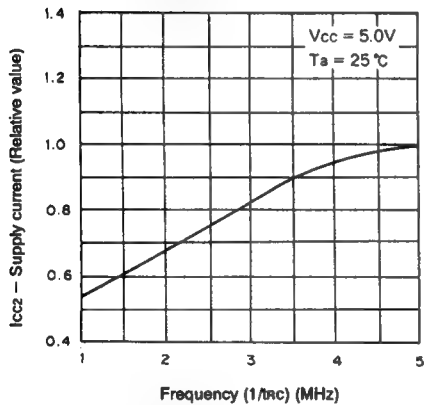
Supply current vs. Supply voltage



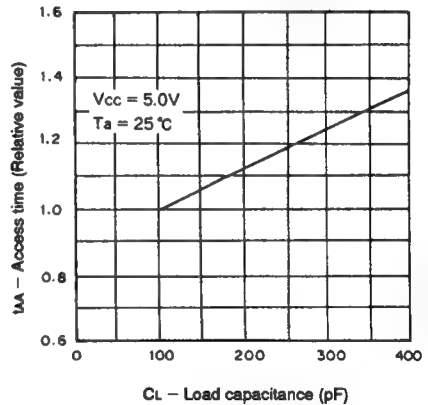
Supply current vs. Ambient temperature



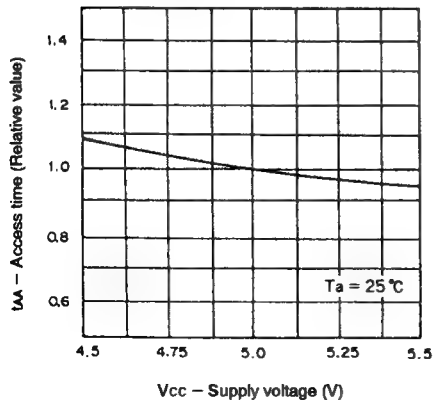
Supply current vs. Frequency



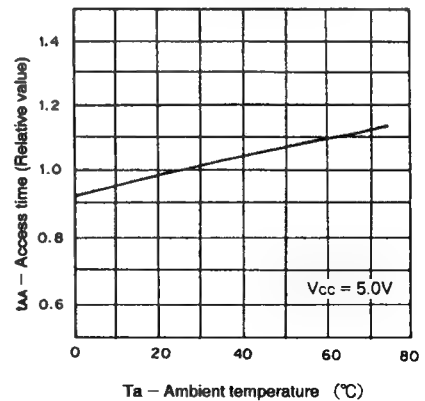
Access time vs. Load capacitance



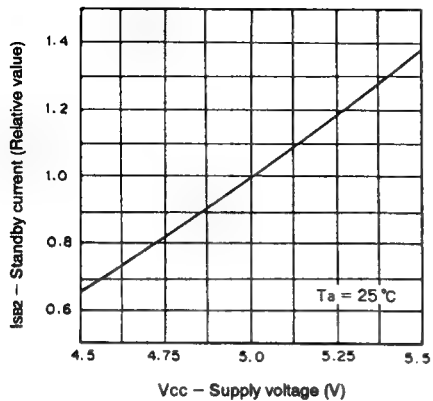
Access time vs. Supply voltage



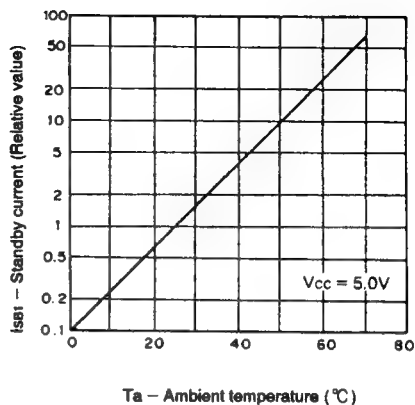
Access time vs. Ambient temperature



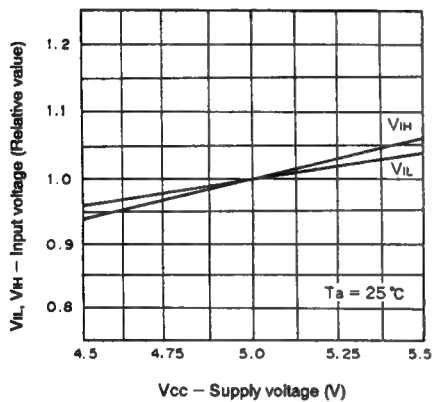
Standby current vs. Supply voltage



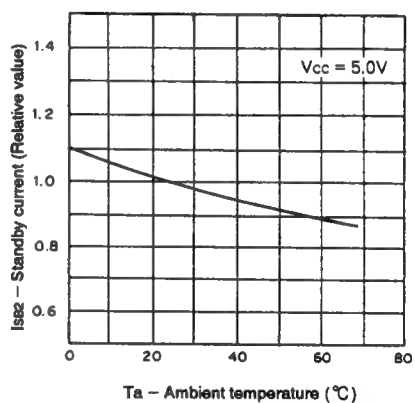
Standby current vs. Ambient temperature



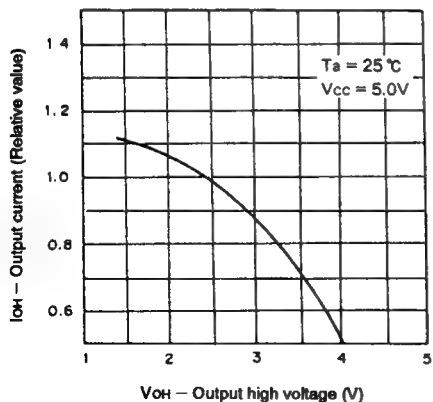
Input voltage level vs. Supply voltage



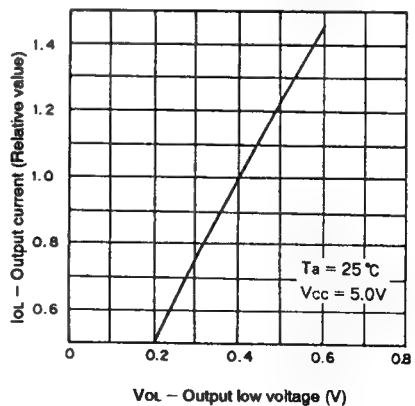
Standby current vs. Ambient temperature



Output current vs. Output voltage

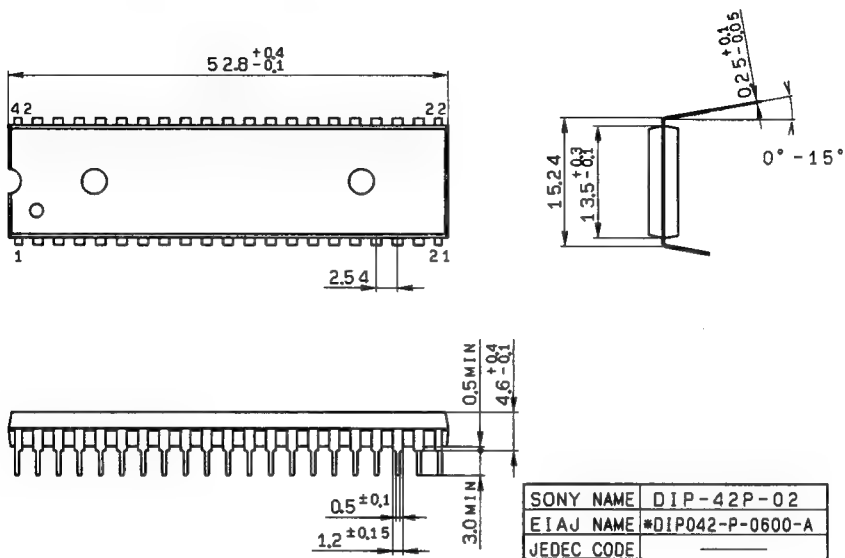


Output current vs. Output voltage

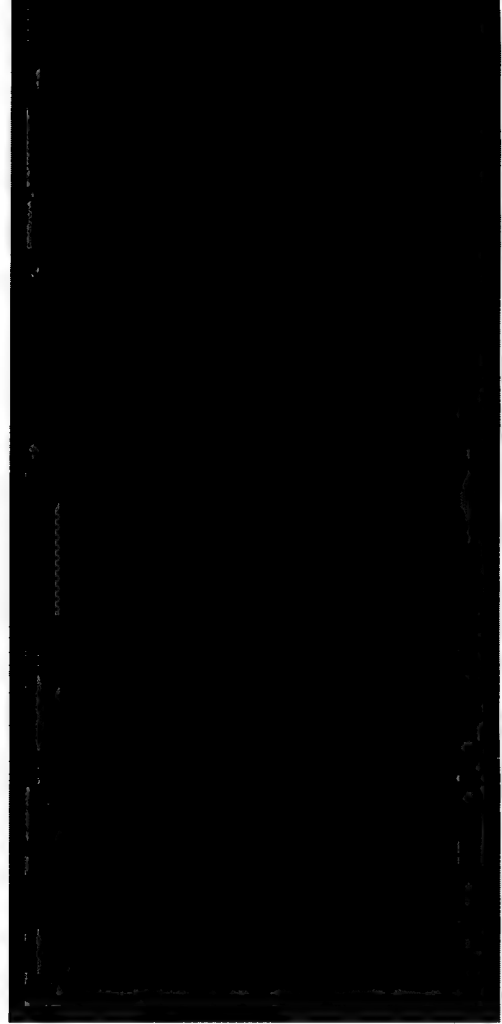


Package Outline Unit : mm

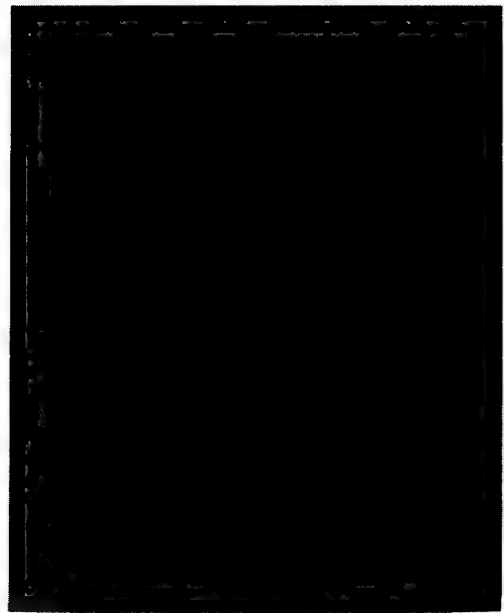
42pin DIP (Plastic) 600mil







Nonvolatile Memories



4) Nonvolatile Memories

• EEPROM

Type	Memory capacity	Functions	Page
CXK1023M CXK1023P	2048bit	256×8bit Serial I/O	401
CXK1024M CXK1024P	2048bit	128×16/256×8bit Serial I/O	409

• EPROM

Type	Memorie capacity	Functions	Access time	Page
CXK27C256DQ	256k bit	32k×8bit	150/200ns	420
CXK27C512DQ	512k bit	64k×8bit	150/200ns	430
CXK27C1000DQ	1M bit	128k×8bit (1M Mask ROM pin compatible)	150/200ns	441
CXK27C1001DQ	1M bit	128K×8bit (JEDEC standard)	150/200ns	451

SONY**CXK1023P/M****2048-bit (256-word×8-bit) Non-volatile Memory****Description**

The CXK1023P/M is a 2048-bit electrically erasable and programmable E² PROM organized as 256-word×8-bit. As serial transmission of the data is performed, it corresponds with the microcomputer serial port. (for the Input/Output)

The CMOS structure allows for low power consumption and high speed operation. Built-in boost and timer circuits permit operation at only a 5V power supply. There is no need for external parts.

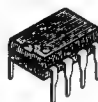
It is most suitable as a non-volatile channel memory for electronic tuners, for use instead of DIP switch, for the setting of various constants and for read only memory systems that require immediate rewrite on the field.

Features

- Structure: 256×8-bit
- Serial data transmission
- Data retention: Over 10 years
- Number of erasures and writings:
Over 10⁵ times
- 3-port control possible
(Connection of DI and DO possible)
- Self time programming cycle (Built-in timer)
- Single 5V power supply
- Low power consumption

During operation	25 mW (Typ.)
During standby	55 μW (Max.)

CXK1023P
8 pin DIP (Plastic)



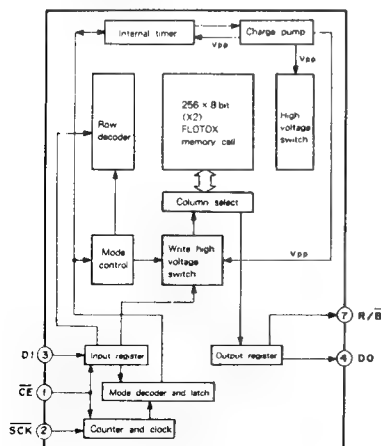
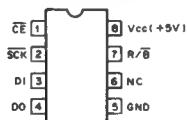
CXK1023M
8 pin SOP (Plastic)

**Function**

256-word×8
Electrically erasable and programmable ROM

Structure

Floating silicon gate CMOS IC

Block Diagram**Pin Configuration
(Top View)****Pin Description**

Symbol	Description
$\overline{\text{CE}}$	Chip enable input
$\overline{\text{SCK}}$	Sync clock
DI	Data input
DO	Data output
GND	Ground
NC	Non connection
R/B	Busy output
Vcc	+5V power supply

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Ratings	Unit
Supply voltage	Vcc	-0.3 to +7.0	V
Input voltage	V _{IH}	-0.3 * to Vcc+0.3	V
Output voltage	V _{IO}	-0.3 * to Vcc+0.3	V
Allowable power dissipation	P _D	0.4	W
Operating temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature * time	T _{solder}	260 * 10	°C * sec

Truth Table

Name	Address	Mode	Data	Function
Read	A ₇ A ₆ A ₅ A ₄ A ₃ A ₂ A ₁ A ₀	1 0 1 0 x x x x	D ₇ to D ₀	(A ₇ -A ₀) Address read
Write	A ₇ A ₆ A ₅ A ₄ A ₃ A ₂ A ₁ A ₀	0 0 1 0 x x x x	D ₇ to D ₀	(A ₇ -A ₀) Address write
Write all bytes	x x x x x x x x	0 1 0 0 x x x x	D ₇ to D ₀	Write all addresses
Status output	x x x x x x x x	0 1 1 0 x x x x	0 (Busy) , 1 (Ready)	Busy flag

Recommended Operating Conditions

(Ta=-20 to +75°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input voltage "H" level	V _{IH}	0.7Vcc	Vcc	Vcc	V
Input voltage "L" level	V _{IL}	0	0	0.3Vcc	V

Electrical Characteristics**• DC characteristics**

(Ta=-20 to +75°C, Vcc=5V ± 10%, GND=0V)

Item	Symbol		Conditions	Min.	Typ.	Max.	Unit
Power supply current	Icc		CE=V _{IL} , t=1MHz, I _{OUT} =0mA *	—	4.5	10	mA
Standby current	I _{SA}		CE, SCK, DI, BYTE Open	—	—	10	μA
Input pull up current	I _{IU}	CE, SCK, DI, BYTE	V _{IN} =0V	-30	-60	-180	μA
Output leak current	I _{OLK}	DO, R/ \bar{B}		—	—	±10	μA
Output voltage "H" level	V _{OH}	DO, R/ \bar{B}	I _{OH} =-400 μA I _{OL} =2.1mA	2.4	—	—	V
Output voltage "L" level	V _{OL}	DO, R/ \bar{B}		—	—	0.4	V

* Including during write operation.

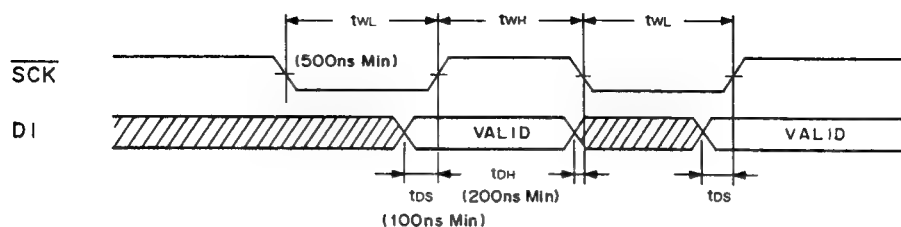
• AC characteristics

(Ta=-20 to +75°C, Vcc=5V ± 10%, GND=0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	t _{WH}		500	—	—	ns
Clock pulse width	t _{WL}		500	—	—	ns
Data input set up time	t _{BS}		100	—	—	ns
Data input hold time	t _{BH}		200	—	—	ns
Chip enable set up time	t _{CES}		100	—	—	ns
Chip enable hold time	t _{CEH}		200	—	—	ns
Clock hold time	t _{CKH}		100	—	—	ns
Clock set up time	t _{CKS}		100	—	—	ns
Data delay time	t _{OD}	DC, C _L =100pF	—	—	400	ns
Program time	t _{PP}		—	8	15	ms
Memory retention time	t _{MH}	After rewriting 10 ⁵ times store at Ta=75°C	10	—	—	Year

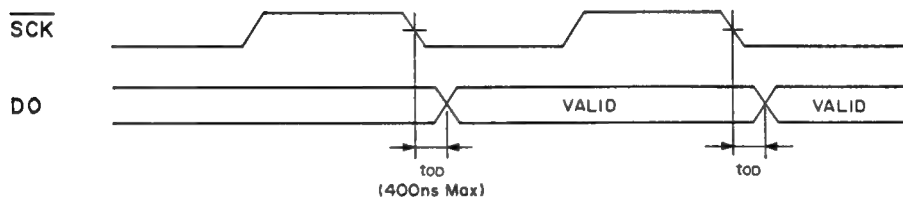
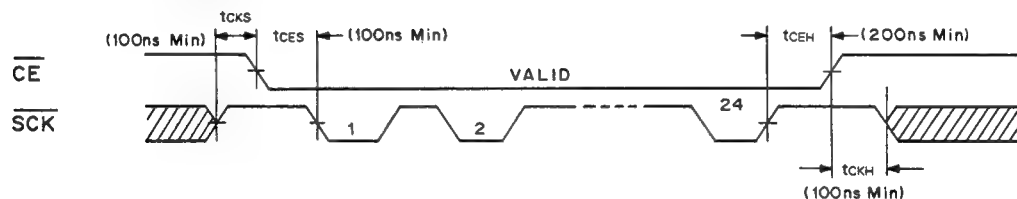
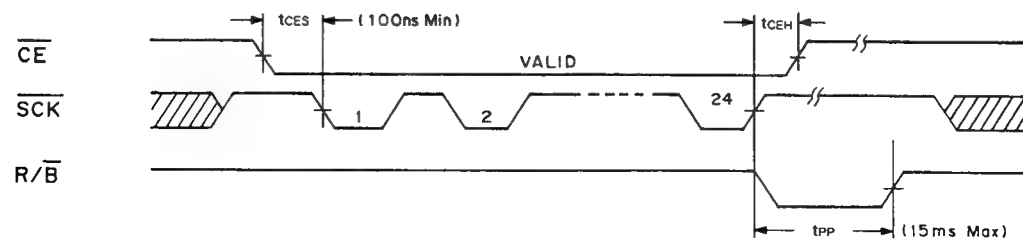
I/O Timing Chart

INPUT MODE



 Unrelated to "H" or "L".

OUTPUT MODE

 \overline{CE} TIMING 1 (DR MODE) \overline{CE} TIMING 2 (DW, ALDW MODE)

Pins Function

- \overline{CE} :**
- ① At "L" the chip is selected. At "H" this pin resets the internal counter. Accordingly, before performing in a mode, turn this pin to "H" once.
 - ② During the execution of write (when busy output is at "L") write is continued regardless of this pin's input.
 - ③ After write completion, read mode becomes possible after turning this pin to "H". Only in status output mode, can this pin be turned to "H" during write execution, and after the internal counter is reset, can read become possible.
- \overline{SCK} :**
- ① With the clock rising edge, input data is read from DI.
 - ② Data is output from DO, synchronously with the clock falling edge.
- DI:**
- ① Data (address, mode, write data) input pin
 - ② DI should be stable 100ns before (t_{DS}) \overline{SCK} rising edge.
- DO:**
- ① Data (read data, status output) output pin
 - ② At high impedance data is not output and connection to DI is possible.
- R/\overline{B} :**
- ① Outputs "L" during write execution.

Description of Operation

For 8-bit mode (BYTE: at H or OPEN)

As the BYTE pin is pulled up, it is fixed to OPEN or "H". In 8-bit mode, input is effected in the order of address data (8-bit) and mode data (4-bit).

① Read: DR (Data Read)

100ns (t_{CES}) or more after \overline{CE} has been turned to L, drop the first clock.

Address data 8-bit and mode data 4-bit (1010) are input. (Data is read with the rising edge of clocks 1 to 12.)

The following 4-bit is dummy data. Synchronously with the falling edge of clock 17, data is output in the order from D_7 to D_0 . 200ns (t_{CEH}) or more after the 24th clock rising edge, turn \overline{CE} to H.

② Write: DW (Data Write)

100ns (t_{CES}) or more after \overline{CE} has been turned to L, drop the first clock.

Address data 8-bit, mode data 4-bit (0010), dummy data 4-bit and data 8-bit (D_7 to D_0), are input. (Data is written with the rising edge of clocks 1 to 24.) Erase and write are executed automatically after the 24th clock rising edge. 200ns (t_{CEH}) or more after the rising edge of clock 24 turn \overline{CE} to H. Within 15ms (T_{pp}) at most, erase and write are completed. During this period as R/\overline{B} pin outputs L, by monitoring R/\overline{B} pin, write completion (L to H) can be detected. Also, by referring to STS mode, shown below, write completion can be detected at DO pin.

③ All Byte Data Write: ALDW

With the input of mode data (0100), the same data (D_7 to D_0) is simultaneously written to all addresses. Address data 8-bit is ignored.

④ Status output: STS

100ns (t_{CES}) or more after \overline{CE} has been turned to L, drop the first clock.

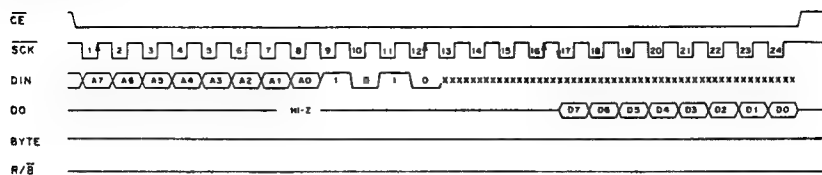
Mode data is input as 0110.

Synchronously with the falling edge of clock 17, L is output from DO pin if it is during write operation, and H, if it is at write completion.

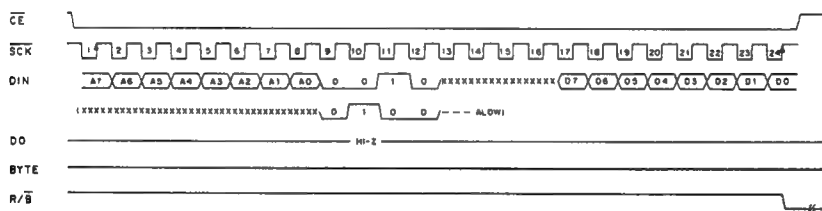
With \overline{CE} at L, the clock is not input and by monitoring DO variation from L to H, write completion can be detected similarly as with R/\overline{B} pin. However during this period, DO keeps on the output of L or H. To turn DO to high impedance condition, it is necessary to turn \overline{CE} to H.

Timing Diagram

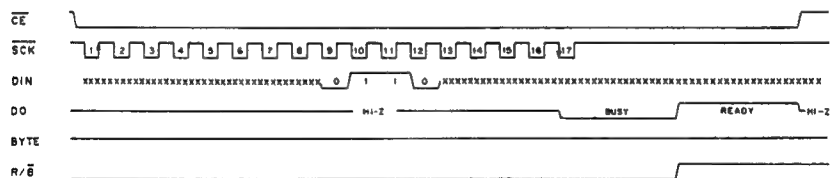
• DR (Data Read)



• DW (Data Write), ALDW (All Byte Data Write)

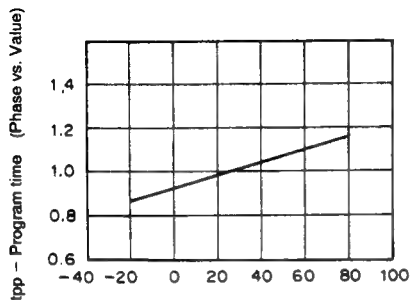


• STS (Status Output)

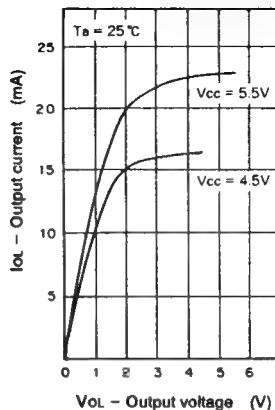


Example of Representative Characteristics

Program time temperature characteristics

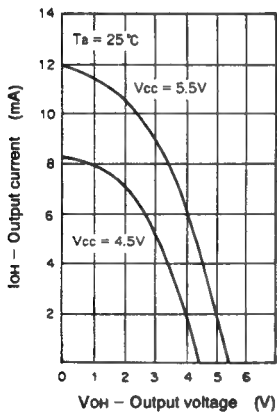
 T_a - Ambient temperature ($^{\circ}\text{C}$)

DO pin output characteristics (Typ.)



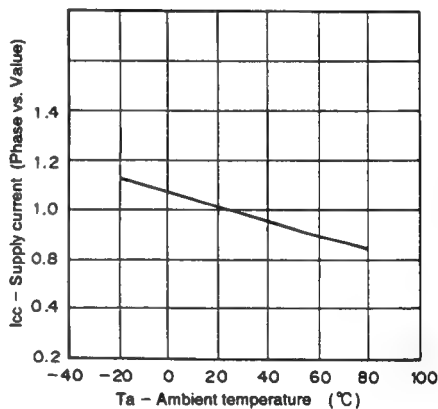
VOL - Output voltage (V)

DO pin output characteristics (Typ.)



VOH - Output voltage (V)

Supply current temperature characteristics

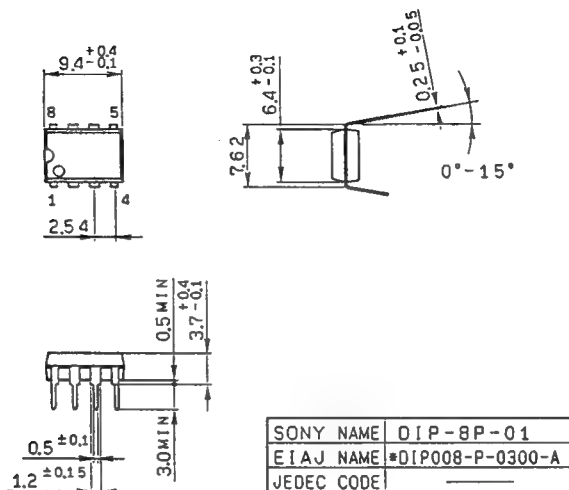
 T_a - Ambient temperature ($^{\circ}\text{C}$)

Package Outline

Unit : mm

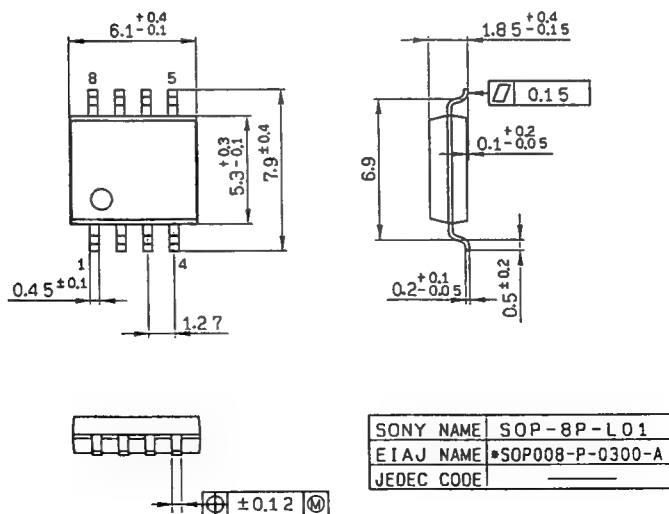
CXK1023P

8pin DIP (Plastic) 300mil 0.5g



CXK1023M

8pin SOP (Plastic) 300mil 0.1g



2048-bit (128-word×16-bit, 256-word×8-bit) Non-volatile Memory
Description

The CXK1024P/M is a 2048-bit electrically erasable and programmable E² PROM organized as 128-word×16-bit or 256-word×8-bit. As serial transmission of the data is performed, it corresponds with the microcomputer serial port. (for the Input/Output)

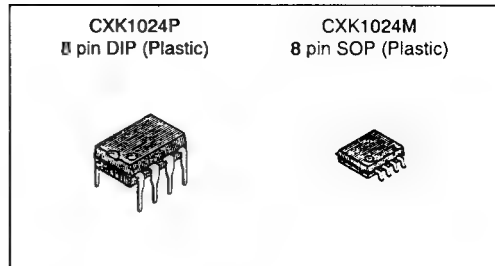
The CMOS structure allows for low power consumption and high speed operation. Built-in boost and timer circuits permit operation at only a 5V power supply. There is no need for external parts.

It is most suitable as a non-volatile channel memory for electronic tuners, for use instead of DIP switch, for the setting of various constants and for read only memory systems that require immediate rewrite on the field.

Features

- Structure: 128×16-bit or 256×8-bit
- Serial data transmission
- Data retention: Over 10 years
- Number of erasures and writings:
Over 10⁵ times
- 3-port control possible
(Connection of DI and DO possible)
- Self time programming cycle (Built-in timer)
- Single 5V power supply
- Low power consumption

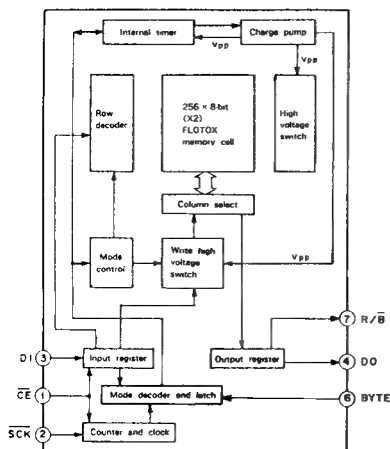
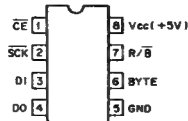
During operation	25	mW (Typ.)
During standby	55	μW (Max.)


Function

128-word×16	} Electrically erasable and programmable ROM
256-word×8	

Structure

Floating silicon gate CMOS IC

Block Diagram

**Pin Configuration
(Top View)**

Pin Description

Symbol	Description
CE	Chip enable input
SCK	Sync clock
DI	Data input
DO	Data output
GND	Ground
BYTE	16/8 bit mode select
R/B	Busy output
Vcc	+5V power supply

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	-0.3 to +7.0	V
Input voltage	V _{IH}	-0.3 * to V _{CC} +0.3	V
Output voltage	V _{I/O}	-0.3 * to V _{CC} +0.3	V
Allowable power dissipation	P _D	0.4	W
Operating temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

Truth Table

1) When BYTE is at L

Data turns to 16-bit mode (128-word × 16-bit). The following functions are available.

Name	Mode	Address	Data	Function
Read	1 0 1 0 1 0 0 0	A ₈ A ₅ A ₄ A ₃ A ₂ A ₁ A ₀ 0	D ₁₅ to D ₈ , D ₇ to D ₀	(A ₈ -A ₀) Address read
Write	1 0 1 0 0 1 0 0	A ₈ A ₅ A ₄ A ₃ A ₂ A ₁ A ₀ 0	D ₁₅ to D ₈ , D ₇ to D ₀	(A ₈ -A ₀) Address write
Write all bytes	× × × × 1 1 0 1	× × × × × × × ×	D ₁₅ to D ₈ , D ₇ to D ₀	Write all addresses
Status output	1 0 1 0 1 0 0 1	0 0 × × × × × ×	0 (Busy), 1 (Ready)	Busy flag

2) When BYTE is at H or OPEN

Data turns to 8-bit mode (256-word × 8-bit). The following functions are available.

Name	Address	Mode	Data	Function
Read	A ₇ A ₆ A ₅ A ₄ A ₃ A ₂ A ₁ A ₀	1 0 1 0 × × × ×	D ₇ to D ₀	(A ₇ -A ₀) Address read
Write	A ₇ A ₆ A ₅ A ₄ A ₃ A ₂ A ₁ A ₀	0 0 1 0 × × × ×	D ₇ to D ₀	(A ₇ -A ₀) Address write
Write all bytes	× × × × × × × ×	0 1 0 0 × × × ×	D ₇ to D ₀	Write all addresses
Status output	× × × × × × × ×	0 1 1 0 × × × ×	0 (Busy), 1 (Ready)	Busy flag

Recommended Operating Conditions

(Ta=-20 to +75°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input voltage "H" level	V _{IH}	0.7V _{CC}	V _{CC}	V _{CC}	V
Input voltage "L" level	V _{IL}	0	0	0.3V _{CC}	V

Electrical Characteristics**• DC characteristics**

(Ta=-20 to +75°C, Vcc=5V ± 10%, GND=0V)

Item	Symbol		Conditions	Min.	Typ.	Max.	Unit
Power supply current	I _{cc}		CE=V _{IL} , t=1MHz, I _{OUT} =0mA *	—	4.5	10	mA
Standby current	I _{ss}		CE, SCK, DI, BYTE Open	—	—	10	μA
Input pull up current	I _{IU}	CE, SCK, DI, BYTE	V _{IN} =0V	-30	-60	-180	μA
Output leak current	I _{OLK}	DO, R/B		—	—	±10	μA
Output voltage "H" level	V _{OH}	DO, R/B	I _{OH} =-400 μA I _{OL} =2.1mA	2.4	—	—	V
Output voltage "L" level	V _{OL}	DO, R/B		—	—	0.4	V

* Including during write operation.

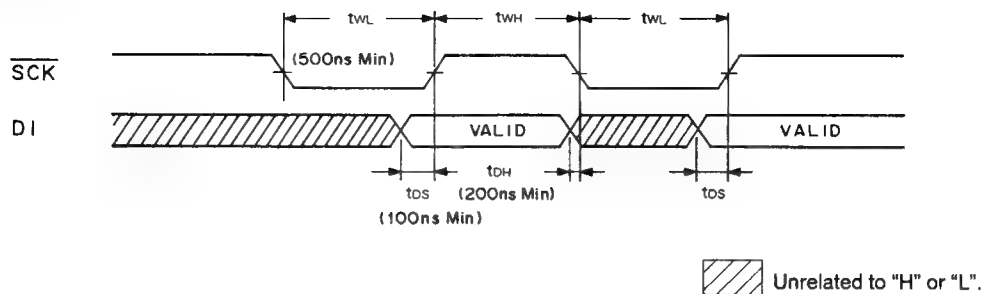
• AC characteristics

(Ta=-20 to +75°C, Vcc=5V ± 10%, GND=0V)

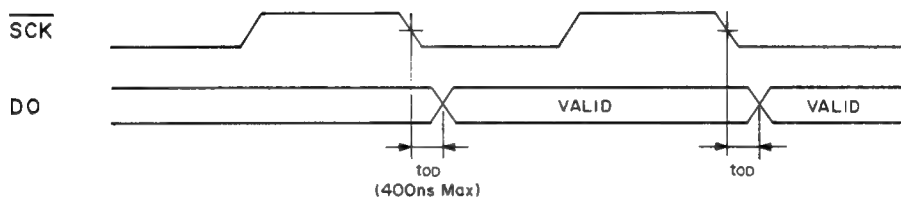
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	t _{WH}		500	—	—	ns
Clock pulse width	t _{WL}		500	—	—	ns
Data input set up time	t _{DS}		100	—	—	ns
Data input hold time	t _{DH}		200	—	—	ns
Chip enable set up time	t _{CES}		100	—	—	ns
Chip enable hold time	t _{CEH}		200	—	—	ns
Clock hold time	t _{CKH}		100	—	—	ns
Clock set up time	t _{CKS}		100	—	—	ns
Data delay time	t _{OD}	DC, C _L =100pF	—	—	400	ns
Program time	t _{PP}		—	8	15	ms
Memory retention time	t _{MH}	After rewriting 10 ⁵ times store at Ta=75°C	10	—	—	Year

I/O Timing Chart

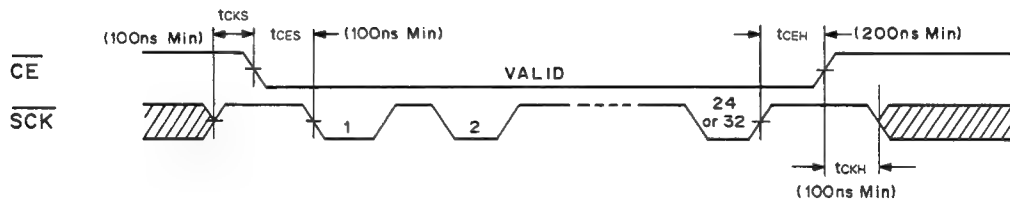
INPUT MODE



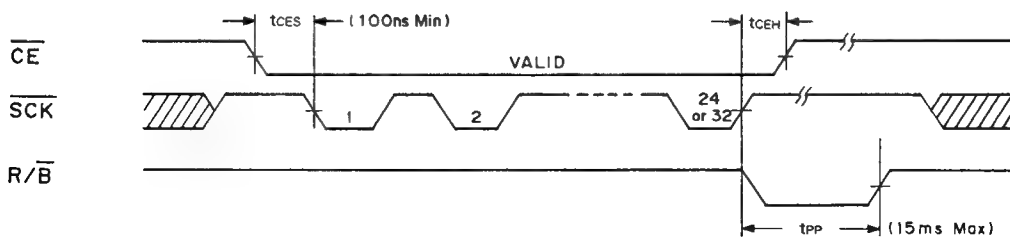
OUTPUT MODE



CE TIMING 1 (DR MODE)



CE TIMING 2 (DW, ALDW MODE)



Pins Function

- \overline{CE} ; ① At "L" the chip is selected. At "H" this pin resets the internal counter. Accordingly, before performing in a mode, turn this pin to "H" once.
② During the execution of write (when busy output is at "L") write is continued regardless of this pin's input.
③ After write completion, read mode becomes possible after turning this pin to "H". Only in status output mode, can this pin be turned to "H" during write execution, and after the internal counter is reset, can read become possible.
- \overline{SCK} ; ① With the clock rising edge, input data is read from DI.
② Data is output from DO, synchronously with the clock falling edge.
- DI; ① Data (address, mode, write data) input pin
② DI should be stable 100ns before (tos) \overline{SCK} rising edge.
- DO; ① Data (read data, status output) output pin
② At high impedance data is not output and connection to DI is possible.
- BYTE; ① This pin specifies whether write and read data are at 16-bit or 8-bit.
② The pull up function makes it turn to 8-bit mode when fixed at OPEN or "H".
③ Fixed at "L", turns to 16-bit mode.
- R/ \overline{B} ; ① Outputs "L" during write execution.

Description of Operation

(1) For the 16-bit mode (BYTE: at L)

BYTE pin is fixed to "L".

For the 16-bit mode, mode data and address data are input in order.

① Read: DR (Data Read)

100ns or more (t_{CES}) after \overline{CE} has been set to L, drop the first clock.

Input is effected from DI in the order of mode data 8-bit (10101000) and address data 7-bit (A_6 to A_0). (Data is read with the rising edge of clocks 1 to 15.) Output is effected synchronously with the falling edge of clock 17 in the order of D_{15} D_{14} ... D_1 D_0 . 200ns (t_{CEH}) or more after the 32nd clock rising edge, turn \overline{CE} to H.

② Write: DW (Data Write)

100ns or more (t_{CES}) after \overline{CE} has been set to L, drop the first block.

Input is effected from DI in the order of mode data 8-bit (10100100), address data 7-bit (A_6 to A_0), dummy bit and data 16-bit (D_{15} to D_0). (Data is read with the rising edge of clocks 1 to 32.) From the rising edge of the 32nd clock, erase and write are executed automatically. 200ns (t_{CEH}) or more from the rising edge of the 32nd clock, turn \overline{CE} to H. With 15ms (T_{pp}) at most, erase and write are completed. During this period, as R/\overline{B} pin outputs L, by monitoring R/\overline{B} pin (L to H), write completion can be detected.

Also, by referring to STS output, shown below, write completion can be detected at DO pin.

③ All Byte Data Write: ALDW

With the input of mode data (XXXX1101), all addresses synchronously write the same data (D_{15} to D_0). (Address data 8-bit is neglected.)

④ Status output: STS (Status)

100ns (t_{CES}) or more after \overline{CE} has been set to L, drop the first block.

Mode data 10-bit (1010100100) is input from DI.

Synchronously with the falling edge of clock 17, L is output from DO pin if it is during write operation, and H, if it is at write completion.

With \overline{CE} at L, the clock is not input and by monitoring DO variation from L to H, write completion can be detected similarly as with R/\overline{B} pin. However during this period, DO keeps on the output of L or H. To turn DO to high impedance condition, it is necessary to turn \overline{CE} to H.

(2) For 8-bit mode (BYTE: at H or OPEN)

As the BYTE pin is pulled up, it is fixed to OPEN or "H". In 8-bit mode, input is effected in the order of address data (8-bit) and mode data (4-bit).

① Read: DR (Data Read)

100ns (t_{CES}) or more after \overline{CE} has been turned to L, drop the first clock.

Address data 8-bit and mode data 4-bit (1010) are input. (Data is read with the rising edge of clocks 1 to 12.) The following 4-bit is dummy data. Synchronously with the falling edge of clock 17, data is output in the order from D_7 to D_0 . 200ns (t_{CEH}) or more after the 24th clock rising edge, turn \overline{CE} to H.

② Write: DW (Data Write)

100ns (t_{ces}) or more after \overline{CE} has been turned to L, drop the first clock.

Address data 8-bit, mode data 4-bit (0010), dummy data 4-bit and data 8-bit (D_7 to D_0), are input. (Data is written with the rising edge of clocks 1 to 24.) Erase and write are executed automatically after the 24th clock rising edge. 200ns (t_{cen}) or more after the rising edge of clock 24 turn \overline{CE} to H. Within 15ms (T_{pp}) at most, erase and write are completed. During this period as R/\overline{B} pin outputs L, by monitoring R/\overline{B} pin, write completion (L to H) can be detected. Also, by referring to STS mode, shown below, write completion can be detected at DO pin.

③ All Byte Data Write: ALDW

With the input of mode data (0100), the same data (D_7 to D_0) is simultaneously written to all addresses. Address data 8-bit is ignored.

④ Status output: STS

100ns (t_{ces}) or more after \overline{CE} has been turned to L, drop the first clock.

Mode data is input as 0110.

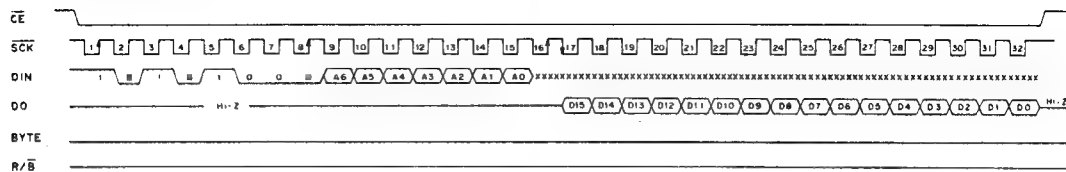
Synchronously with the falling edge of clock 17, L is output from DO pin if it is during write operation, and H, if it is at write completion.

With \overline{CE} at L, the clock is not input and by monitoring DO variation from L to H, write completion can be detected similarly as with R/\overline{B} pin. However during this period, DO keeps on the output of L or H. To turn DO to high impedance condition, it is necessary to turn \overline{CE} to H.

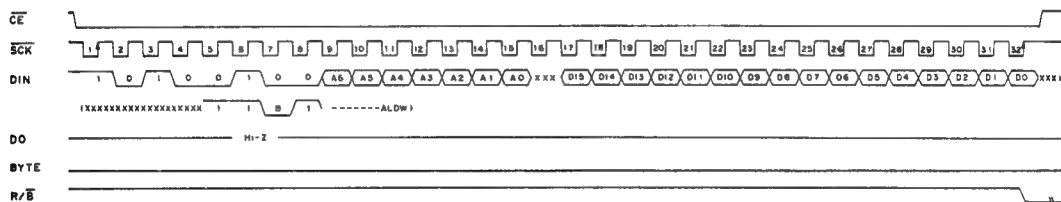
Timing Diagram

1) 16-bit mode

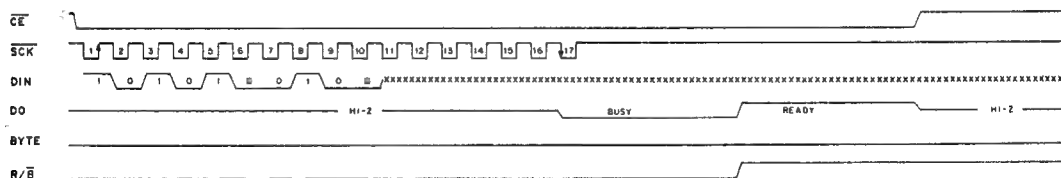
• DR (Data Read)



• DW (Data Write), ALDW (All Byte Data Write)

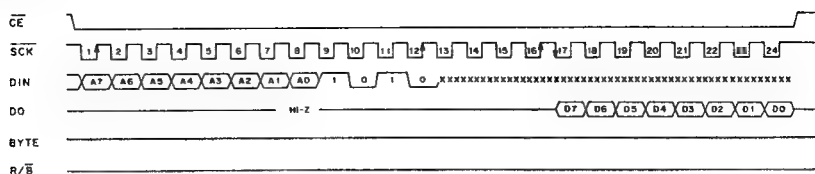


• STS (Status Output)

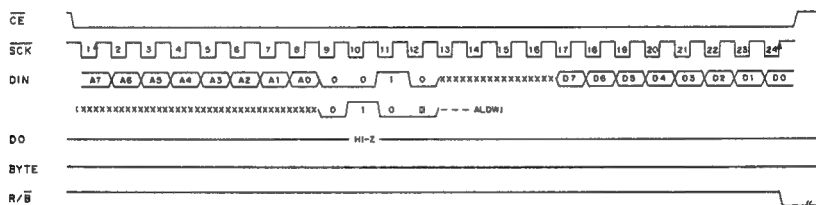


2) 8-bit mode

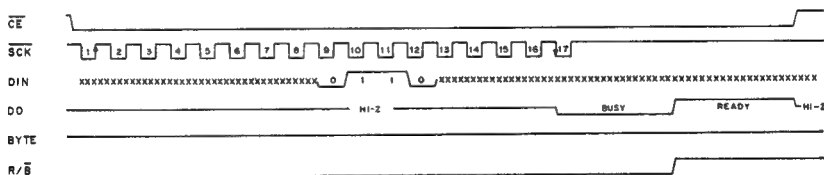
• DR (Data Read)



• DW (Data Write), ALDW (All Byte Data Write)

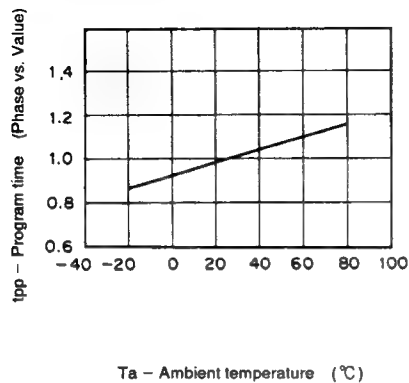


• STS (Status Output)

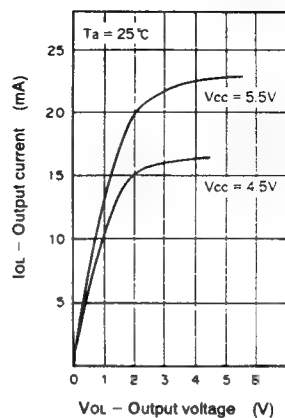


Example of Representative Characteristics

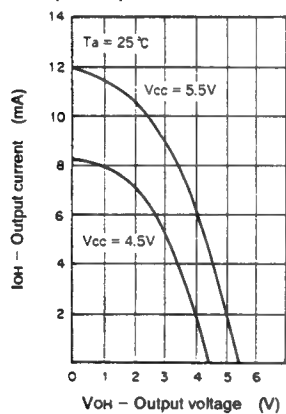
Program time temperature characteristics



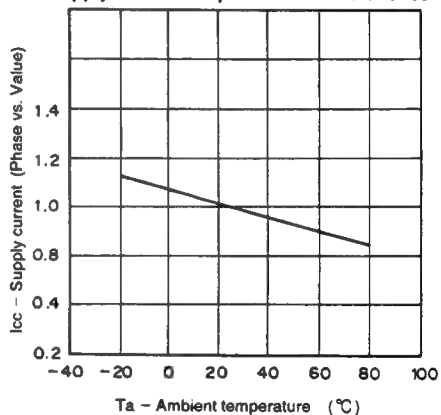
DO pin output characteristics (Typ.)



DO pin output characteristics (Typ.)



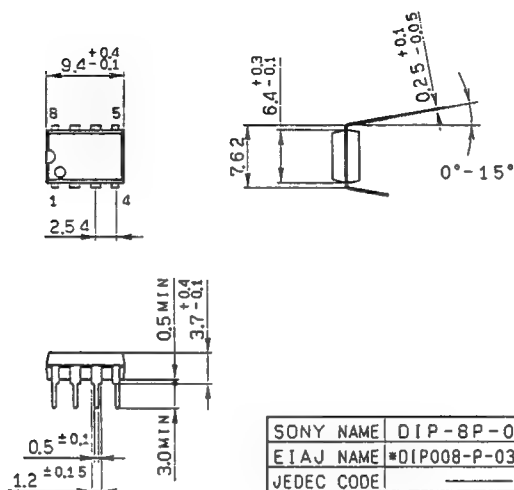
Supply current temperature characteristics



Package Outline Unit : mm

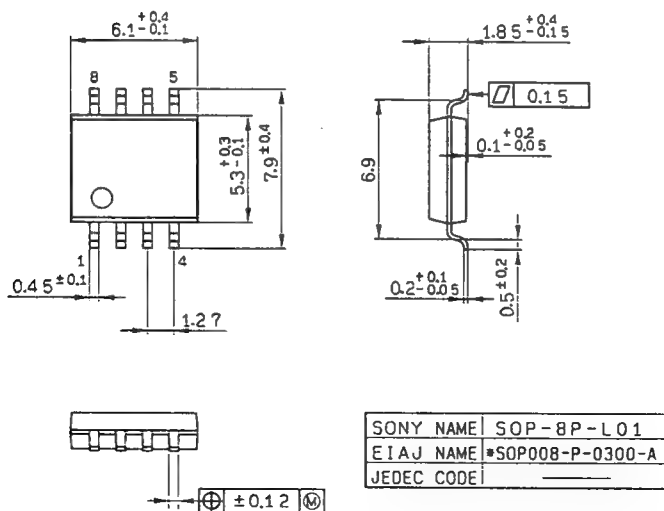
CXK1024P

8pin DIP (Plastic) 300mil 0.5g



CXK1024M

8pin SOP (Plastic) 300mil 0.1g



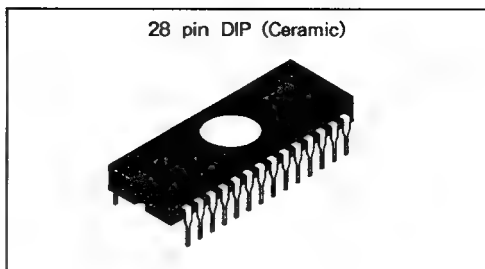
32768-word × 8-bit Ultraviolet Erasable CMOS EPROM

Description

The CXK27C256DQ is an electrically programmable, ultraviolet erasable CMOS EPROM. The adoption of CMOS for the peripheral circuits allows for high speed operation and low power consumption. Ideally suited for 8-bit micro-processor systems requiring large program memories, this IC is organized as 32768-word by 8-bit in a 28 pin Frit-Seal package.

Features

- Fast access time : (Access time)
CXK27C256DQ-15 150ns (Max.)
CXK27C256DQ-20 200ns (Max.)
- Low current consumption
at operation current 50mA (Max.)
at standby 1mA (Max.)
- At read out 5V single supply operation :
5V ± 10 %
- Directly TTL compatible :
All inputs and outputs
- 3-state output
- High speed program mode
- 600-mil 28 pin ceramic DIP package



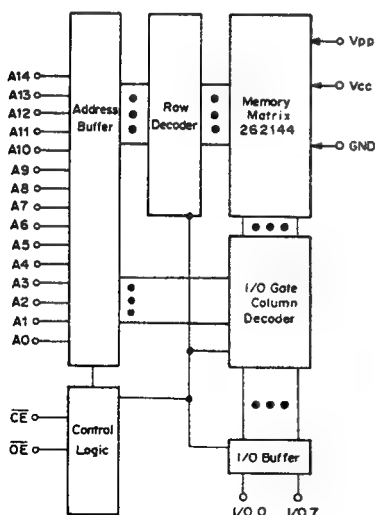
Function

32768-word × 8-bit EPROM

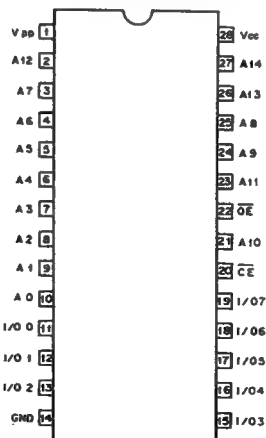
Structure

Silicon Stacked-gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O 0 to I/O 7	Data I/O
\overline{CE}	Chip enable input
\overline{OE}	Output enable input
Vpp	Program power supply
Vcc	+ 5V power supply
GND	GND

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	Vcc	− 0.6 to + 7.0	V
	Vpp	− 0.6 to + 14	V
Input voltage	A9	− 0.6 to + 13.5	V
	V _{IN}	− 0.6 to + 6.5	V
Output voltage	V _{I/O}	− 0.6 to + 6.5	V
Operating temperature	Topr	− 10 to + 80	°C
Storage temperature	Tstg	− 65 to + 125	°C

Exposure to stress exceeding the Absolute Maximum Ratings may not only adversely affect reliability but at the worst, destroy the device.

Truth Table

\overline{CE}	\overline{OE}	A9	Vpp	Mode	I/O pin
L	L	X	Vcc	Read	Data output
L	H	X	Vcc	Output disable	High impedance
H	X	X	Vcc	Standby	High impedance
L	X	X	Vpp	Program	Data input
L	L	X	Vpp	Program verify	Data output
H	X	X	Vpp	Program inhibit	High impedance
L	L	V _H	Vcc	Electronic signature	Device code output

Set X to either "H" or "L", V_H = 12V ± 0.5V

Read Mode**Recommended Operating Conditions**

(Ta = 0 to + 70°C, GND = 0V, Vpp = Vcc*)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.0	—	Vcc + 0.5	V
Input low voltage	V _{IL}	− 0.1	—	0.8	V

* Vpp must be applied simultaneously or after Vcc and removed simultaneously or before Vcc.

Electrical Characteristics

• DC characteristics

(V_{CC} = 5V ± 10 %, V_{pp} = V_{CC}, GND = 0V, T_a = 0 to +70 °C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = 5.5V	-10	—	10	μA
Output leakage current	I _{LO}	V _{I/O} = 5.5V	-10	—	10	μA
V _{CC} average operating supply current	I _{CC1}	Cycle time 90ns Duty = 100 % I _{OUT} = 0mA CE = OE = V _{IL}	—	—	50	mA
V _{CC} standby supply current	I _{SB}	CE = V _{IH}	—	—	1	mA
V _{pp} supply current	I _{pp1}		—	—	0.1	mA
Output high voltage	V _{OH}	I _{OH} = -400 μA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.45	V

* V_{CC} = 5V, T_a = 25 °C

I/O capacitance

(T_a = 25 °C, f = 1MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	4	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	12	pF

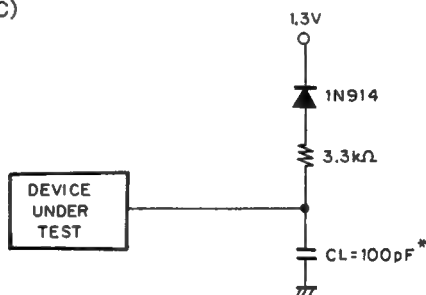
Note) This parameter is sampled and is not 100 % tested.

AC characteristics

• AC test conditions

(V_{CC} = 5V ± 10 %, V_{pp} = V_{CC}, T_a = 0 to +70 °C)

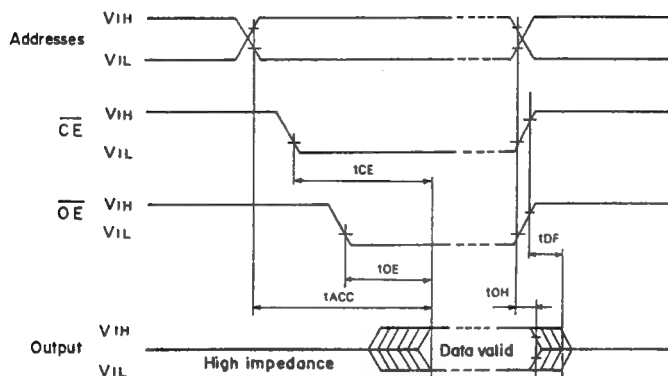
Item	Conditions
Input pulse high voltage	V _{IH} = 2.4V
Input pulse low voltage	V _{IL} = 0.45V
Input rise time	tr ≤ 20ns
Input fall time	tf ≤ 20ns
I/O reference level	2V/0.8V
Load condition	Right figure

* C_L includes scope and jig capacitances.

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Address access time	t_{ACC}	—	150	—	200	ns
Chip enable access time	t_{CE}	—	150	—	200	ns
Output enable access time	t_{OE}	—	65	—	70	ns
Output data hold time	t_{OH}	0	—	0	—	ns
Output disable time	t_{DF}^*	0	50	0	60	ns

* t_{DF} is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100% tested.

Timing Waveform (Read cycle)



Programming Operation**Recommended Operating Conditions**

(Ta = 25 ± 5°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Vcc supply voltage	Vcc*1	6.00	6.25	6.50	V
Vpp program supply voltage	Vpp*2	12.50	12.75	13.00	V
Input high voltage	VIH	2.0		Vcc + 0.5V	V
Input low voltage	VIL	-0.1		0.8	V

*1 Vcc must be applied before Vpp and removed after Vpp.

*2 Keep Vpp below 14V including overshoot.

Extraction of the device while 12.75V is applied to Vpp may impair reliability.

Electrical Characteristics**• DC characteristics**

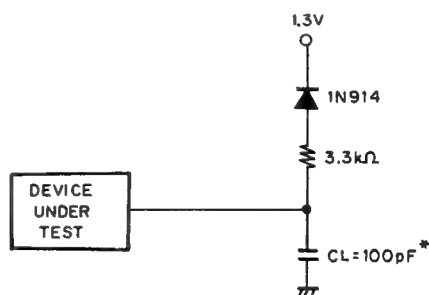
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input leakage current	ILI	VIN = VIL or VIH	-10	—	10	μA
Vcc supply current	Icc2		—	—	50	mA
Vpp supply current	Ipp2	$\overline{CE} = V_{IL}$	—	—	50	mA
Output high voltage (at verify)	VOH	IOH = -400 μA	2.4	—	—	V
Output low voltage (at verify)	VOL	IOL = 2.1mA	—	—	0.45	V
A9 electronic signature	VID		11.5	12.0	12.5	V

AC Characteristics**• AC test conditions**

(Vcc = 6.25 ± 0.25V, Vpp = 12.75 ± 0.25V, Ta = 20 to +30°C)

Item	Conditions
Input pulse high voltage	VIH = 2.4V
Input pulse low voltage	VIL = 0.45V
Input rise time	tr ≤ 20ns
Input fall time	tf ≤ 20ns
I/O reference level	2V/0.8V
Load conditions	Right figure

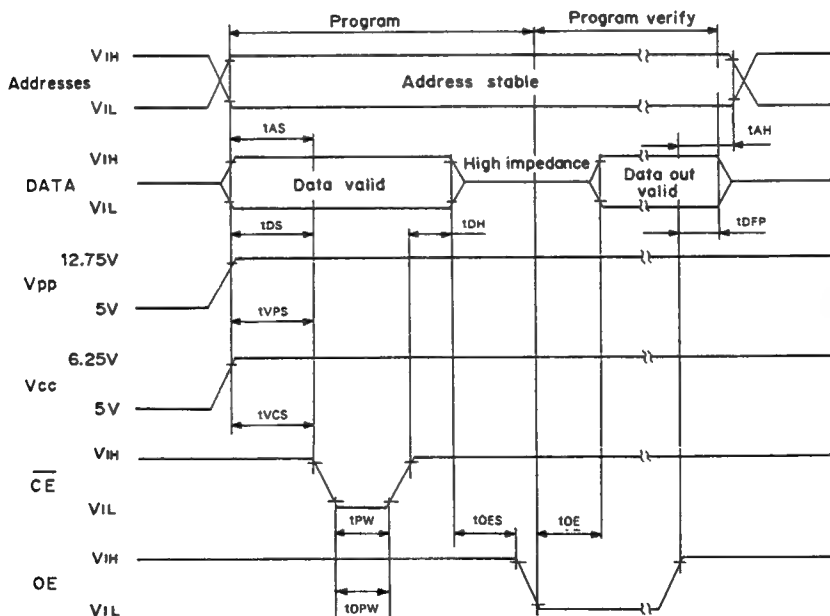
* CL includes scope and jig capacitances.



Item	Symbol	Min.	Max.	Unit
Address setup time	tAS	2		μ s
$\overline{\text{OE}}$ setup time	tOES	2		μ s
Data setup time	tDS	2		μ s
Address hold time	tAH	0		μ s
Data hold time	tDH	2		μ s
$\overline{\text{OE}}$ high to output float delay	tDFP*	0	130	ns
Vpp setup time	tVPS	2		μ s
Vcc setup time	tVCS	2		μ s
$\overline{\text{CE}}$ setup time	tCES	2		μ s
Program pulse width	tPW	95	105	μ s
Data valid from $\overline{\text{OE}}$	tOE		100	ns

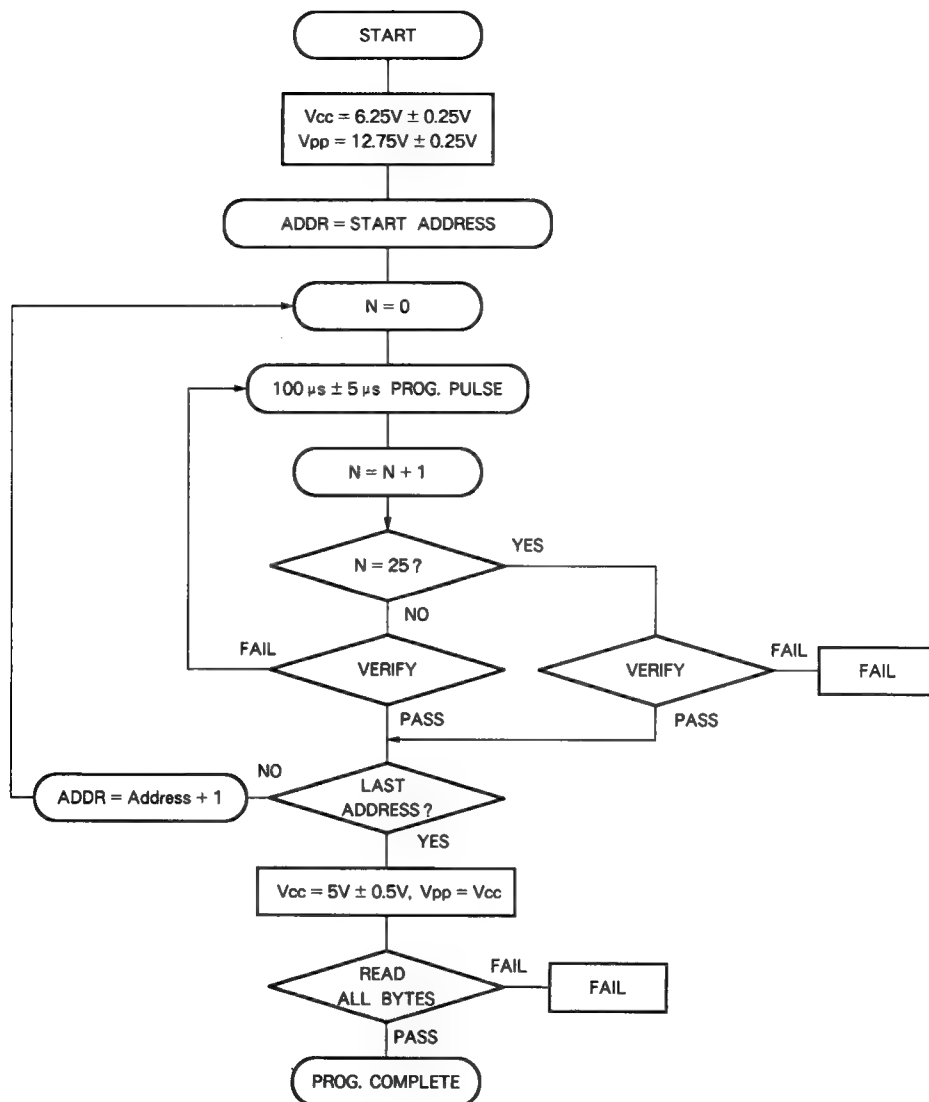
* tDFP is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100% tested.

Timing Waveform (Program)



Note) When programming the CXK27C256DQ a 0.1 μ F capacitor is required across Vpp and GND to suppress switching noise caused by Vpp transient current.

High Speed Programming Method Flow Chart



Erase Operation

The recommended erasure procedure for the CXK27C256DQ ("0" to "1") is exposure to ultraviolet light of a 2537 Å wavelength through the translucent window. The exposure dose (i.e. UV intensity X exposure time) for erasure should be at a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with an illuminance of 12000 µW/cm² on the package surface placed within 2 to 3cm of the lamp tubes. Moreover, erasure may require larger periods according to the ultraviolet lamp life and the dirt on the quartz window.

In this IC, erasure of data starts when exposed to light with a wavelength of 4000 Å or less. Considering that sunlight and some fluorescent lighting contain elements of a wavelength between 3000 and 4000 Å, long usage under such type of lighting conditions calls for protection. In such cases, use an opaque seal and the like to cover the glass window and prevent chip exposure to light.

Operation Modes**Read Mode**

This IC features a chip enable (\overline{CE}) and an output enable (\overline{OE}). \overline{CE} selects the device and at the same time controls the power down function. \overline{OE} controls the output buffer, independently from \overline{CE} . By setting the address while $\overline{CE} = \overline{OE} = V_{IL}$, data becomes stable after t_{ACC} .

After address has become stable, respective data become stable when after t_{CE} , \overline{CE} is lowered to V_{IL} from V_{IH} in $\overline{OE} = V_{IL}$ condition, or \overline{OE} is lowered from V_{IH} to V_{IL} in $\overline{CE} = V_{IL}$ condition, after t_{OE} .

Output Disable Mode

By turning \overline{OE} to V_{IH} , the output pin turns to high impedance condition irrespectively of other inputs. This function completely prevents bus contention and allows for an easy connection of several devices on a common bus line.

Standby Mode

Turning \overline{CE} to V_{IH} automatically brings in power down condition. Then current consumption I_{CC} is reduced to a maximum 1mA. Also, output turns to high impedance condition irrespectively of \overline{OE} .

Notes on Operation

Supply current I_{CC} features 3 levels depending on the device operating condition. Standby current level, operating current level and transient peak current level. The transient peak current is the source of switching noise and the cause of high speed IC's misoperation. As the magnitude of the transient peak current heavily depends on the inductance and capacitance of the output load. This can be suppressed through the usage of a decoupling capacitor.

When the system is built, it is recommended to insert a high frequency 1 µF ceramic capacitor between V_{CC} and GND on every device, and as close to the device as possible.

In addition, a 4.7 µF electrolytic capacitor is recommended for every 8 devices. This should be close to the power supply to overcome voltage drop caused by the PCB wiring inductance.

Program Mode

When delivered, and after each erasure, all bits of the CXK27C256DQ are in the "1" state (Output "H" level). Data is introduced by selectively programming "0s" (output "L" level). To change a "0" to a "1" by ultraviolet light erasure is necessary. (See article on UV Erasure.)

The CXK27C256DQ is set to programming mode when 12.75V is applied to Vpp pin, "L" level to \overline{CE} and "H" level to \overline{OE} .

High Speed Programming Method

During programming and verify operation a circuit that automatically monitors the programming of cells is activated. Thus over program pulse so far in use is not necessary, and programming time is greatly reduced to 13 seconds.

Program Inhibit Mode

By turning Vpp to 12.75V, \overline{CE} to V_{IH} and $\overline{OE} = V_{IH}$, programming is inhibited. Using this mode allows for programming of multiple devices in parallel with different data. With the input of $\overline{CE} = V_{IL}$ pulse into the device selected for programming, this can be performed independently from other devices.

Program Verify

To verify if programming has been correctly performed at the specified address, memory cells are read out. Data of the selected address is output by turning to $\overline{CE} = V_{IH}$ and $\overline{OE} = V_{IL}$ at Vpp = 12.75V.

Electronic Signature Mode

Electronic signature serves to identify the manufacturer and the device type of each EPROM. This function is intended for use by the programming equipment to automatically match the device to be programmed with its corresponding programming algorithm.

At read mode, 12V is applied to address A9.

A1 to A8, A10 to A14 = $\overline{OE} = \overline{CE} = V_{IL}$ is obtained.

With A0 = V_{IL} the manufacturer code is output and with A0 = V_{IH} the device code is output.

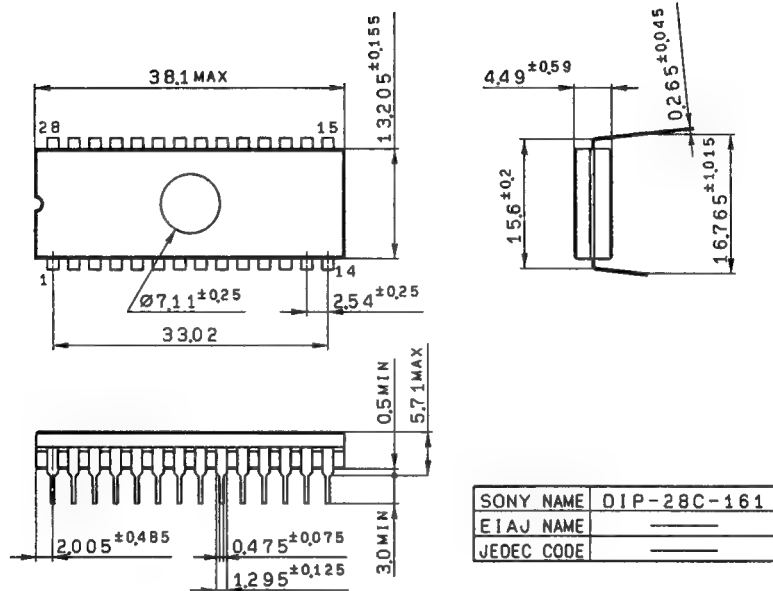
The chart below shows the Electronic Signature.

Signature \ Pins	A0	07	06	05	04	03	02	01	00	Hex
Manufacturer Code	V_{IL}	0	0	1	0	0	0	0	0	20
Device Code	V_{IH}	1	0	0	0	1	1	0	1	8D

Package Outline

Unit : mm

28 pin DIP (Ceramic)



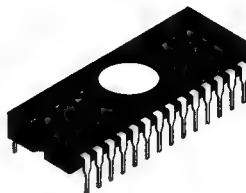
SONY**CXK27C512DQ** -15/20**65536-word × 8-bit Ultraviolet Erasable CMOS EPROM****Description**

The CXK27C512DQ is an electrically programmable, ultraviolet erasable CMOS EPROM. The adoption of CMOS for the peripheral circuits allows for high speed operation and low power consumption. Ideally suited for 8-bit micro-processor systems requiring large program memories, this IC is organized as 65536-word by 8-bit in a 28 pin Frit-Seal package.

Features

- Fast access time : (Access time)
CXK27C512DQ-15 150ns (Max.)
CXK27C512DQ-20 200ns (Max.)
- Low current consumption
at operation current 50mA (Max.)
at standby 1mA (Max.)
- At read out 5V single supply operation :
5V ± 10 %
- Directly TTL compatible :
All inputs and outputs
- 3-state output
- High speed program mode
- 600-mil 28 pin ceramic DIP package

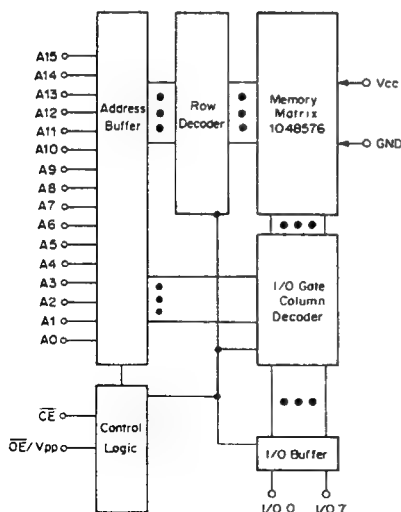
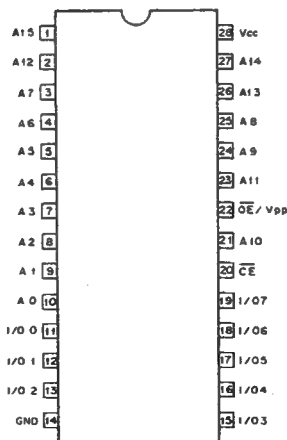
28 pin DIP (Ceramic)

**Function**

65536-word × 8-bit EPROM

Structure

Silicon Stacked-gate CMOS IC

Block Diagram**Pin Configuration
(Top View)****Pin Description**

Symbol	Description
A0 to A15	Address input
I/O0 to I/O7	Data I/O
\overline{CE}	Chip enable input
\overline{OE}/V_{pp}	Output enable input/Program power supply
Vcc	+ 5V power supply
GND	GND

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	- 0.6 to + 7.0	V
	V _{PP}	- 0.6 to + 14	V
Input voltage	A ₉	- 0.6 to + 13.5	V
	V _{IN}	- 0.6 to + 6.5	V
Output voltage	V _{I/O}	- 0.6 to + 6.5	V
Operating temperature	T _{opr}	- 10 to + 80	°C
Storage temperature	T _{stg}	- 65 to + 125	°C

Exposure to stress exceeding the Absolute Maximum Ratings may not only adversely affect reliability but at the worst, destroy the device.

Truth Table

CE	OE/ V _{PP}	A ₉	Mode	I/O pin
L	L	X	Read	Data output
L	H	X	Output disable	High impedance
H	X	X	Standby	High impedance
L	V _{PP}	X	Program	Data input
H	V _{PP}	X	Program inhibit	High impedance
L	L	V _H	Electronic signature	Device code output

Set X to either "H" or "L", V_H = 12V ± 0.5V

Read Mode**Recommended Operating Conditions**(Ta = 0 to + 70°C, GND = 0V, V_{PP} = V_{CC}*)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.0	—	V _{CC} + 0.5	V
Input low voltage	V _{IL}	- 0.1	—	0.8	V

* V_{PP} must be applied simultaneously or after V_{CC} and removed simultaneously or before V_{CC}.

Electrical Characteristics**• DC characteristics**(V_{CC} = 5V ± 10%, V_{pp} = V_{CC}, GND = 0V, T_a = 0 to +70°C)

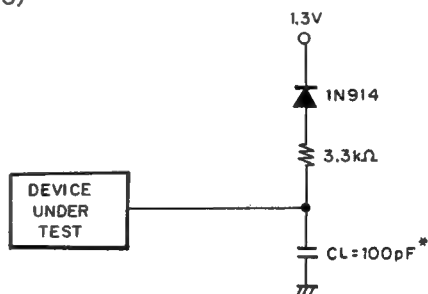
Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = 5.5V	-10	—	10	μA
Output leakage current	I _{LO}	V _{I/O} = 5.5V	-10	—	10	μA
V _{CC} average operating supply current	I _{CC1}	Cycle time 100ns Duty = 100 % I _{OUT} = 0mA $\overline{CE} = \overline{OE} = V_{IL}$	—	—	50	mA
V _{CC} standby supply current	I _{SB}	$\overline{CE} = V_{IH}$	—	—	1	mA
V _{pp} supply current	I _{pp1}		—	—	0.1	mA
Output high voltage	V _{OH}	I _{OH} = -400 μA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.45	V

* V_{CC} = 5V, T_a = 25°C**I/O capacitance**(T_a = 25°C, f = 1MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	4	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	12	pF

Note) This parameter is sampled and is not 100% tested.**AC characteristics****• AC test conditions**(V_{CC} = 5V ± 10%, V_{pp} = V_{CC}, T_a = 0 to +70°C)

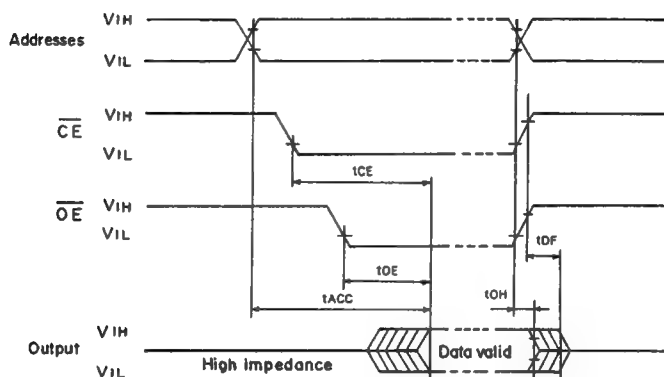
Item	Conditions
Input pulse high voltage	V _{IH} = 2.4V
Input pulse low voltage	V _{IL} = 0.45V
Input rise time	t _r ≤ 20ns
Input fall time	t _f ≤ 20ns
I/O reference level	2V/0.8V
Load condition	Right figure

* C_L includes scope and jig capacitances.

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Address access time	t_{ACC}	—	150	—	200	ns
Chip enable access time	t_{CE}	—	150	—	200	ns
Output enable access time	t_{OE}	—	60	—	70	ns
Output data hold time	t_{OH}	0	—	0	—	ns
Output disable time	t_{DF}^*	0	50	0	60	ns

* t_{DF} is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100% tested.

Timing Waveform (Read cycle)



Programming Operation**Recommended Operating Conditions**

(Ta = 25 ± 5°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Vcc supply voltage	Vcc*1	6.00	6.25	6.50	V
Vpp program supply voltage	Vpp*2	12.50	12.75	13.00	V
Input high voltage	VIH	2.0		Vcc + 0.5V	V
Input low voltage	VIL	-0.1		0.8	V

*1 Vcc must be applied before Vpp and removed after Vpp.

*2 Keep Vpp below 14V including overshoot.

Extraction of the device while 12.75V is applied to Vpp may impair reliability.

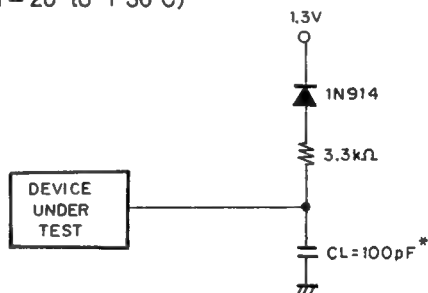
Electrical Characteristics**• DC characteristics**

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input leakage current	II1	VIN = VIL or VIH	-10	—	10	μA
Vcc supply current	Icc2		—	—	50	mA
Vpp supply current	Ipp2	CE = VIL	—	—	50	mA
Output high voltage (at verify)	VOH	IOH = -400 μA	2.4	—	—	V
Output low voltage (at verify)	VOL	IOL = 2.1mA	—	—	0.45	V
A9 electronic signature	VID		11.5	12.0	12.5	V

AC Characteristics**• AC test conditions**

(Vcc = 6.25 ± 0.25V, Vpp = 12.75 ± 0.25V, Ta = 20 to +30°C)

Item	Conditions
Input pulse high voltage	VIH = 2.4V
Input pulse low voltage	VIL = 0.45V
Input rise time	tr ≤ 20ns
Input fall time	tf ≤ 20ns
I/O reference level	2V/0.8V
Load conditions	Right figure

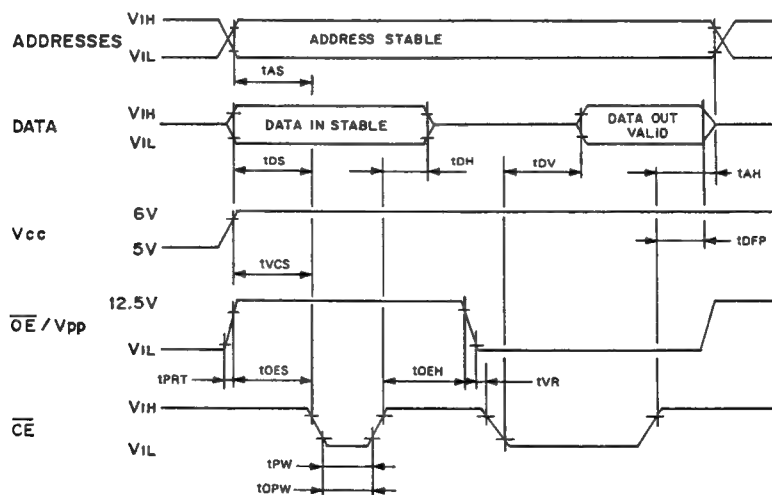


* CL includes scope and jig capacitances.

Item	Symbol	Min.	Max.	Unit
Address setup time	t _{AS}	2		μs
$\overline{\text{OE}}$ setup time	t _{OES}	2		μs
$\overline{\text{OE}}/\text{V}_{\text{pp}}$ hold time	t _{OEH}	2		μs
Data setup time	t _{DS}	2		μs
Address hold time	t _{AH}	0		μs
Data hold time	t _{DH}	2		μs
$\overline{\text{OE}}$ high to output float delay	t _{DFF} *	0	130	ns
V _{CC} setup time	t _{VCS}	0		μs
Program pulse width	t _{PW}	95	105	μs
Data valid from $\overline{\text{CE}}$	t _{DV}		1	ns
$\overline{\text{OE}}/\text{V}_{\text{pp}}$ recovery time	t _{VR}	2		μs
$\overline{\text{OE}}/\text{V}_{\text{pp}}$ pulse rise time	t _{PRT}	50		ns

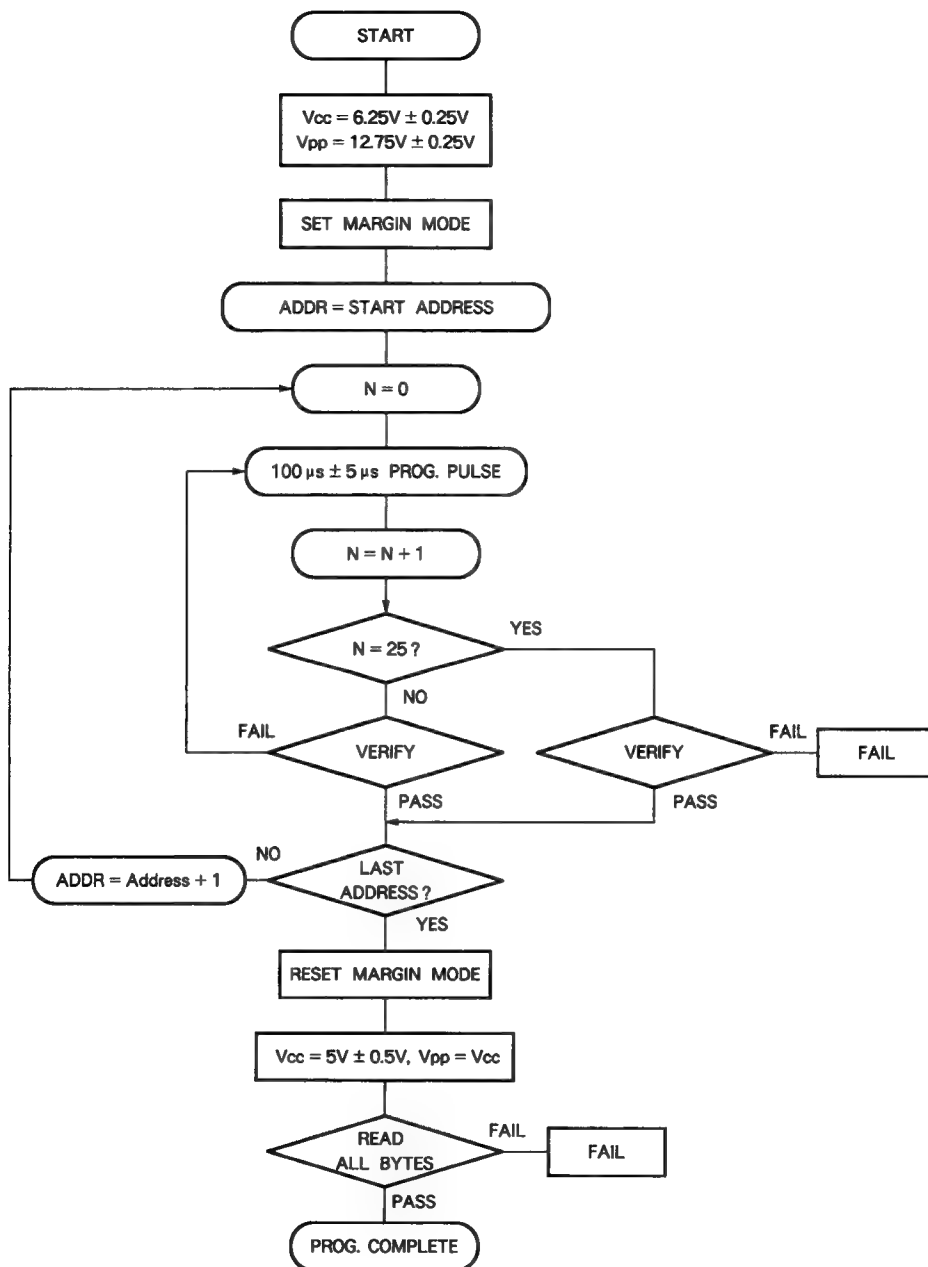
* t_{DFF} is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100 % tested.

Timing Waveform (Program)



Note) When programming the CXK27C512DQ a 0.1 μF capacitor is required across $\overline{\text{OE}}/\text{V}_{\text{pp}}$ and GND to suppress switching noise caused by V_{pp} transient current.

High Speed Programming Method Flow Chart



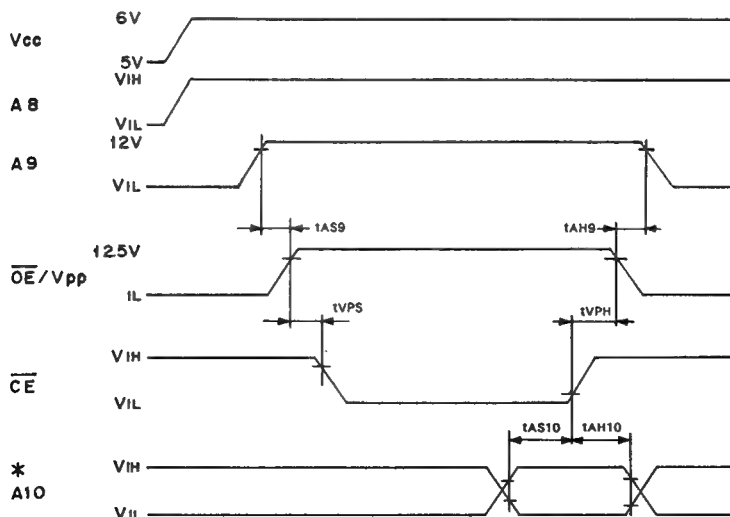
Erase Operation

The recommended erasure procedure for the CXK27C512DQ ("0" to "1") is exposure to ultraviolet light of a 2537 Å wavelength through the translucent window. The exposure dose (i.e. UV intensity X exposure time) for erasure should be at a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with an illuminance of 12000 µW/cm² on the package surface placed within 2 to 3cm of the lamp tubes. Moreover, erasure may require larger periods according to the ultraviolet lamp life and the dirt on the quartz window.

In this IC, erasure of data starts when exposed to light with a wavelength of 4000 Å or less. Considering that sunlight and some fluorescent lighting contain elements of a wavelength between 3000 and 4000 Å, long usage under such type of lighting conditions calls for protection. In such cases, use an opaque seal and the like to cover the glass window and prevent chip exposure to light.

Margin Mode**• AC Characteristics**

Item	Symbol	Min.	Typ.	Max.	Unit
A10 setup time	tAS10	1			µs
A10 hold time	tAH10	1			µs
Vpp hold time	tVPH	2			µs
Vpp setup time	tVPS	2			µs
A9 setup time	tAS9	2			µs
A9 hold time	tAH9	2			µs

Timing Waveform (Margin mode set • reset)

* Set margin mode A10 = VIH, Reset margin mode A10 = VIL.

Operation Modes

Read Mode

This IC features a chip enable (\overline{CE}) and an output enable (\overline{OE}/V_{pp}). \overline{CE} selects the device and at the same time controls the power down function. \overline{OE}/V_{pp} controls the output buffer, independently from \overline{CE} . By setting the address while $\overline{CE} = \overline{OE}/V_{pp} = V_{IL}$, data becomes stable after t_{ACC} .

After address has become stable, respective data become stable when after t_{CE} , \overline{CE} is lowered to V_{IL} from V_{IH} in $\overline{OE}/V_{pp} = V_{IL}$ condition, or \overline{OE}/V_{pp} is lowered from V_{IH} to V_{IL} in $\overline{CE} = V_{IL}$ condition, after t_{OE} .

Output Disable Mode

By turning \overline{OE}/V_{pp} to V_{IH} , the output pin turns to high impedance condition irrespectively of other inputs. This function completely prevents bus contention and allows for an easy connection of several devices on a common bus line.

Standby Mode

Turning \overline{CE} to V_{IH} automatically brings in power down condition. Then current consumption I_{CC} is reduced to a maximum 1mA. Also, output turns to high impedance condition irrespectively of \overline{OE}/V_{pp} .

Notes on Operation

Supply current I_{CC} features 3 levels depending on the device operating condition. Standby current level, operating current level and transient peak current level. The transient peak current is the source of switching noise and the cause of high speed IC's misoperation. As the magnitude of the transient peak current heavily depends on the inductance and capacitance of the output load. This can be suppressed through the usage of a decoupling capacitor.

When the system is built, it is recommended to insert a high frequency 1 μ F ceramic capacitor between V_{CC} and GND on every device, and as close to the device as possible.

In addition, a 4.7 μ F electrolytic capacitor is recommended for every 8 devices. This should be close to the power supply to overcome voltage drop caused by the PCB wiring inductance.

Program Mode

When delivered, and after each erasure, all bits of the CXK27C512DQ are in the "1" state (Output "H" level). Data is introduced by selectively programming "0s" (output "L" level). To change a "0" to a "1" by ultraviolet light erasure is necessary. (See article on UV Erasure.)

The CXK27C512DQ is set to programming mode when 12.75V is applied to \overline{OE}/V_{pp} pin and "L" level to \overline{CE} .

High Speed Programming Method

During programming and verify operation a circuit that automatically monitors the programming of cells is activated. Thus over program pulse so far in use is not necessary, and programming time is greatly reduced to 6 seconds.

Margin Mode

The CXK27C512DQ has margin mode circuit to guarantee sufficient programming margin. Thus over program pulse so far in use is not necessary. If setting this margin mode at programming, sufficient programming margin can be obtained within less than 6 seconds programming time.

Program Inhibit Mode

By turning \overline{OE}/V_{pp} to 12.75V and \overline{CE} to V_{IH} , programming is inhibited. Using this method allows for programming of multiple devices in parallel with different data. With the exception of \overline{CE} wiring is common. With the input of $\overline{CE} = V_{IL}$ pulse into the device selected for programming, this can be performed independently from other devices.

Program Verify

To verify if programming has been correctly performed at the specified address, memory cells are read out. Data of the selected address is output by turning to $\overline{CE} = \overline{OE}/V_{pp} = V_{IL}$.

Electronic Signature Mode

Electronic signature serves to identify the manufacturer and the device type of each EPROM. This function is intended for use by the programming equipment to automatically match the device to be programmed with its corresponding programming algorithm.

At read mode, 12V is applied to address A9.

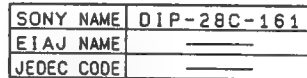
A₁ to A₈, A₁₀ to A₁₅ = $\overline{OE}/V_{pp} = \overline{CE} = V_{IL}$ is obtained.

With A₀ = V_{IL} the manufacturer code is output and with A₀ = V_{IH} the device code is output.

The chart below shows the Electronic Signature.

Signature \ Pins	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer Code	V_{IL}	0	0	1	0	0	0	0	0	20
Device Code	V_{IH}	0	0	1	1	1	1	0	1	3D

28pin DIP (Ceramic)



131072-word × 8-bit Ultraviolet Erasable CMOS EPROM

Description

The CXK27C1000DQ is an electrically programmable, ultraviolet erasable CMOS EPROM. The adoption of CMOS for the peripheral circuits allows for high speed operation and low power consumption. Ideally suited for 8-bit micro-processor systems requiring large program memories, this IC is organized as 131072-word by 8-bit in a 32 pin Frit-Seal package.

This IC has features of pin compatibility with 1M bit mask ROM.

Features

- Fast access time : (Access time)
CXK27C1000DQ-15 150ns (Max.)
CXK27C1000DQ-20 200ns (Max.)
- Low current consumption
at operation current 50mA (Max.)
at standby 1mA (Max.)
- At read out 5V single supply operation : 5V ± 10 %
- Directory TTL compatible : All inputs and outputs
- 3-state output
- High speed program mode
- 600-mil 32 pin ceramic DIP package

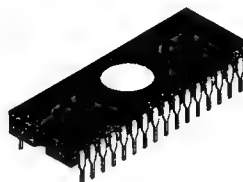
Function

131072-word × 8-bit EPROM

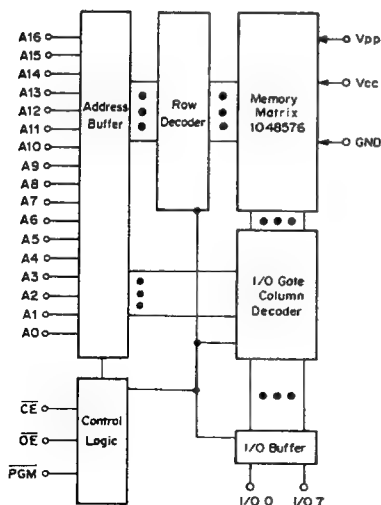
Structure

Silicon Stacked-gate CMOS IC

32 pin DIP (Ceramic)

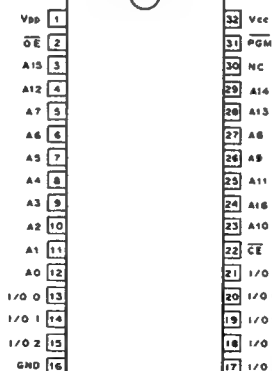


Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O0 to I/O7	Data I/O
CE	Chip enable input
OE	Output enable input
PGM	Program enable input
Vpp	Program power supply
Vcc	+ 5V power supply
GND	GND
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	Vcc	- 0.6 to + 7.0	V
	Vpp	- 0.6 to + 14	V
Input voltage	A9	- 0.6 to + 13.5	V
	V _{IN}	- 0.6 to + 6.5	V
Output voltage	V _{I/O}	- 0.6 to + 6.5	V
Operating temperature	Topr	- 10 to + 80	°C
Storage temperature	Tstg	- 65 to + 125	°C

Exposure to stress exceeding the Absolute Maximum Ratings may not only adversely affect reliability but at the worst, destroy the device.

Truth Table

\overline{CE}	\overline{OE}	A9	PGM	Vpp	Mode	I/O pin
L	L	X	X	Vcc	Read	Data output
L	H	X	X	Vcc	Output disable	High impedance
H	X	X	X	Vcc	Standby	High impedance
L	X	X	L	Vpp	Program	Data input
L	L	X	H	Vpp	Program verify	Data output
H	X	X	X	Vpp	Program inhibit	High impedance
L	L	V _H	H	Vcc	Electronic signature	Device code output

Set X to either "H" or "L", V_H = 12V ± 0.5V

Read Mode**Recommended Operating Conditions**

(Ta = 0 to + 70°C, GND = 0V, Vpp = Vcc*)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.0	—	Vcc + 0.5	V
Input low voltage	V _{IL}	- 0.1	—	0.8	V

* Vpp must be applied simultaneously or after Vcc and removed simultaneously or before Vcc.

Electrical Characteristics

• DC characteristics

(V_{CC} = 5V ± 10%, V_{PP} = V_{CC}, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = 5.5V	-10	—	10	μA
Output leakage current	I _{LO}	V _{I/O} = 5.5V	-10	—	10	μA
V _{CC} average operating supply current	I _{CC1}	Cycle time 125ns Duty = 100 % I _{OUT} = 0mA $\overline{CE} = \overline{OE} = V_{IL}$	—	—	50	mA
V _{CC} standby supply current	I _{SB}	$\overline{CE} = V_{IH}$	—	—	1	mA
V _{PP} supply current	I _{PP1}		—	—	0.1	mA
Output high voltage	V _{OH}	I _{OH} = -400 μA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.45	V

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	4	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	12	pF

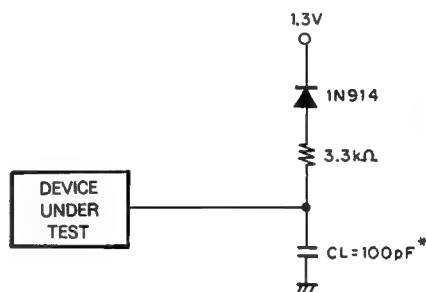
Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions

(V_{CC} = 5V ± 10%, V_{PP} = V_{CC}, T_a = 0 to +70°C)

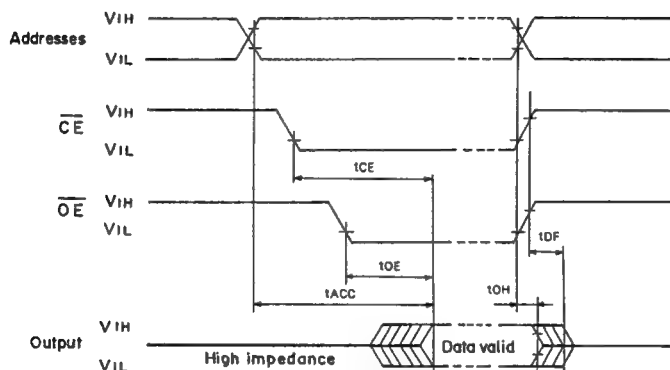
Item	Conditions
Input pulse high voltage	V _{IH} = 2.4V
Input pulse low voltage	V _{IL} = 0.45V
Input rise time	t _r ≤ 20ns
Input fall time	t _f ≤ 20ns
Input reference level	2V/0.8V
Output reference level	2V/0.8V
Load condition	Right figure

* C_L includes scope and jig capacitances.

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Address access time	t_{ACC}	—	150	—	200	ns
Chip enable access time	t_{CE}	—	150	—	200	ns
Output enable access time	t_{OE}	—	65	—	70	ns
Output data hold time	t_{OH}	0	—	0	—	ns
Output disable time	t_{DF}^*	0	50	0	60	ns

* t_{DF} is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100% tested.

Timing Waveform (Read cycle)



Programming Operation**Recommended Operating Conditions**

(Ta = 25 ± 5°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Vcc supply voltage	Vcc*1	6.00	6.25	6.50	V
Vpp program supply voltage	Vpp*2	12.50	12.75	13.00	V
Input high voltage	V _{IH}	2.0		Vcc + 0.5V	V
Input low voltage	V _{IL}	-0.1		0.8	V

*1 Vcc must be applied before Vpp and removed after Vpp.

*2 Keep Vpp below 14V including overshoot.

Extraction of the device while 12.75V is applied to Vpp may impair reliability.

Electrical Characteristics**• DC characteristics**

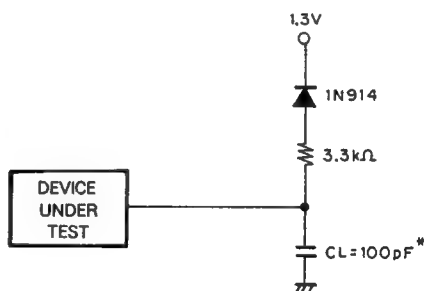
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = V _{IL} or V _{IH}	-10	—	10	μA
Vcc supply current	Icc2		—	—	50	mA
Vpp supply current	Ipp2	$\overline{CE} = V_{IL}$	—	—	50	mA
Output high voltage (at verify)	V _{OH}	I _{OH} = -400 μA	2.4	—	—	V
Output low voltage (at verify)	V _{OL}	I _{OL} = 2.1 mA	—	—	0.45	V
A9 electronic signature	V _{ID}		11.5	12.0	12.5	V

AC Characteristics**• AC test conditions**

(Vcc = 6.25 ± 0.25V, Vpp = 12.75 ± 0.25V, Ta = 20 to +30°C)

Item	Conditions
Input pulse high voltage	V _{IH} = 2.4V
Input pulse low voltage	V _{IL} = 0.45V
Input rise time	tr ≤ 20ns
Input fall time	tf ≤ 20ns
Input reference level	2V/0.8V
Output reference level	2V/0.8V
Load conditions	Right figure

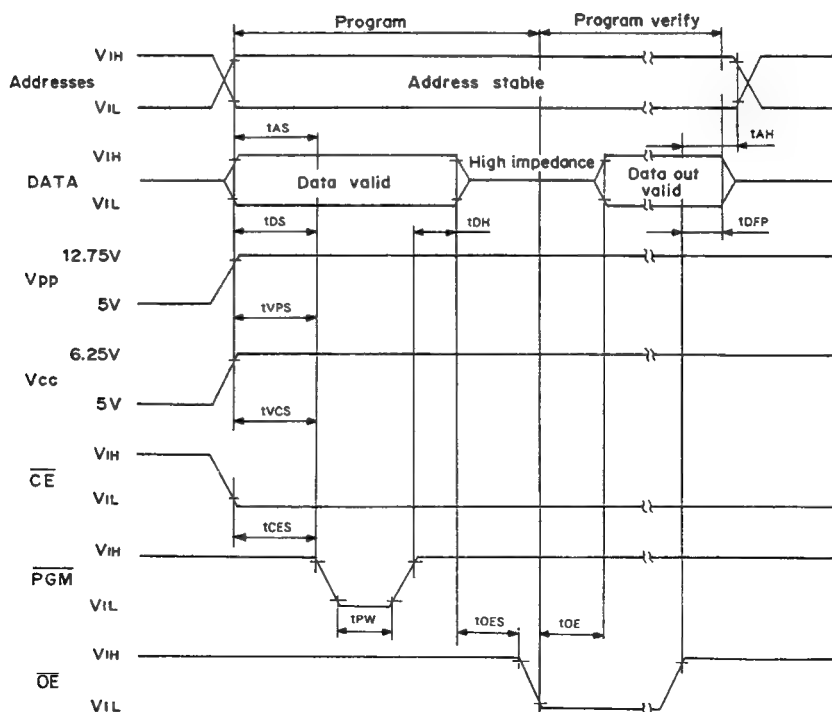
* CL includes scope and jig capacitances.



Item	Symbol	Min.	Max.	Unit
Address setup time	tAS	2		μs
$\overline{\text{OE}}$ setup time	tOES	2		μs
Data setup time	tDS	2		μs
Address hold time	tAH	0		μs
Data hold time	tDH	2		μs
$\overline{\text{OE}}$ high to output float delay	tDFP*	0	130	ns
Vpp setup time	tVPS	2		μs
Vcc setup time	tVCS	2		μs
$\overline{\text{CE}}$ setup time	tCES	2		μs
Program pulse width	tpw	95	105	μs
Data valid from $\overline{\text{OE}}$	tOE		100	ns

* tDFP is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100% tested.

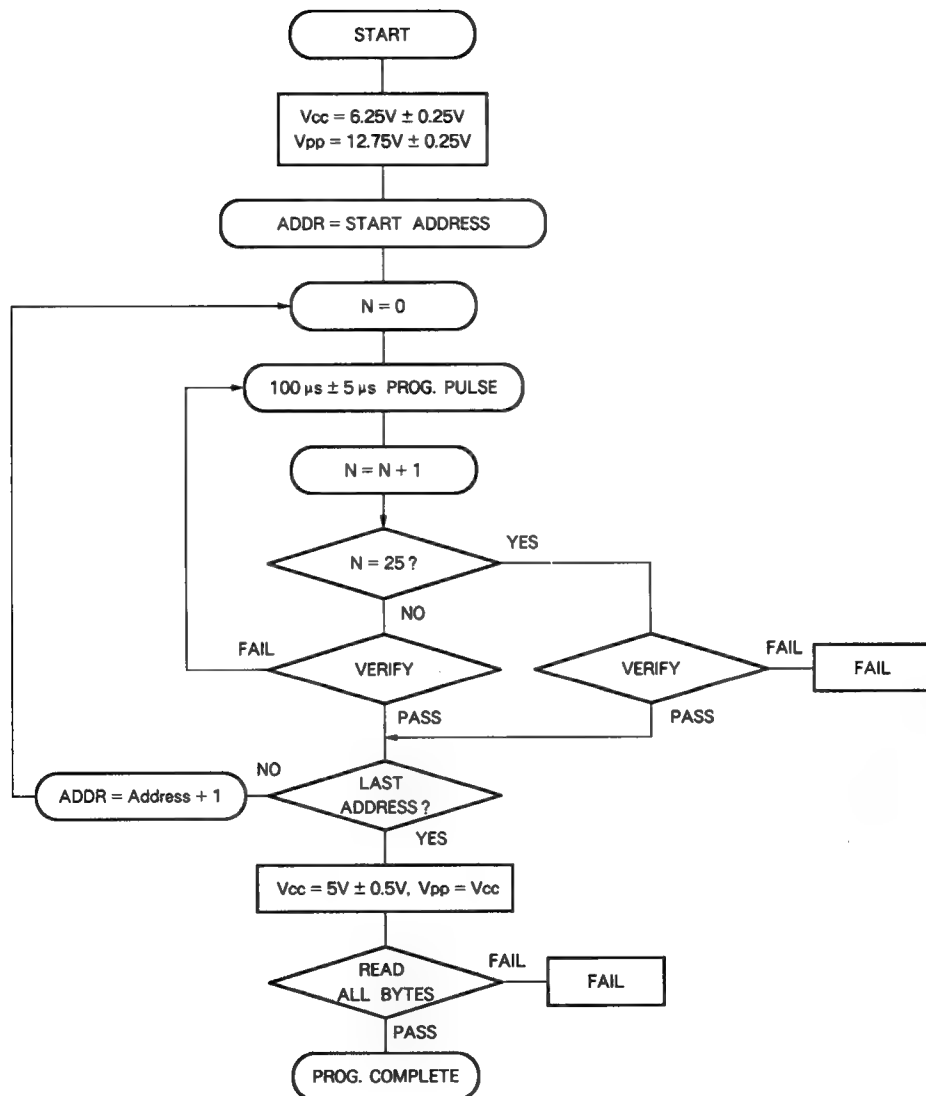
Timing Waveform (Program)



Note) When programming the CXK27C1000DQ a 0.1 μF capacitor is required access Vpp and GND to suppress switching noise caused by Vpp transient current.

High Speed Programming Method Flow Chart

Flowchart



Erase Operation

The recommended erasure procedure for the CXK27C1000DQ ("0" to "1") is exposure to ultraviolet light of a 2537 Å wavelength through the translucent window. The exposure dose (i.e. UV intensity X exposure time) for erasure should be at a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with an illuminance of 12000 µW/cm² on the package surface placed within 2 to 3cm of the lamp tubes. Moreover, erasure may require larger periods according to the ultraviolet lamp life and the dirt on the quartz window.

In this IC, erasure of data starts when exposed to light with a wavelength of 4000 Å or less. Considering that sunlight and some fluorescent lighting contain elements of a wavelength between 3000 and 4000 Å, long usage under such type of lighting conditions calls for protection. In such cases, use an opaque seal and the like to cover the glass window and prevent chip exposure to light.

Operation Modes**Read Mode**

This IC features a chip enable (\overline{CE}) and an output enable (\overline{OE}). \overline{CE} selects the device and at the same time controls the power down function. \overline{OE} controls the output buffer, independently from \overline{CE} . By setting the address while $\overline{CE} = \overline{OE} = V_{IL}$, data becomes stable after t_{ACC} .

After address has become stable, respective data become stable when after t_{CE} , \overline{CE} is lowered to V_{IL} from V_{IH} in $\overline{OE} = V_{IL}$ condition, or \overline{OE} is lowered from V_{IH} to V_{IL} in $\overline{CE} = V_{IL}$ condition, after t_{OE} .

Output Disable Mode

By turning \overline{OE} to V_{IH} , the output pin turns to high impedance condition irrespectively of other inputs. This function completely prevents bus contention and allows for an easy connection of several devices on a common bus line.

Standby Mode

Turning \overline{CE} to V_{IH} automatically brings in power down condition. Then consumption current I_{CC} is reduced to a maximum 1mA. Also, output turns to high impedance condition irrespectively of \overline{OE} .

Notes on Operation

Supply current I_{CC} features 3 levels depending on the device operating condition. Standby current level, operating current level and transient peak current level. The transient peak current is the source of switching noise and the cause of high speed IC's misoperation. As the magnitude of the transient peak current heavily depends on the inductance and capacitance of the output load. This can be suppressed through the usage of a decoupling capacitor.

When the system is built, it is recommended to insert a high frequency 1 µF ceramic capacitor between V_{CC} and GND on every device, and as close to the device as possible.

In addition, a 4.7 µF electrolytic capacitor is recommended for every B devices. This should be close to the power supply to overcome voltage drop caused by the PCB wiring inductance.

Program Mode

When delivered, and after each erasure, all bits of the CXK27C1000DQ are in the "1" state (Output "H" level). Data is introduced by selectively programming "0s" (output "L" level). To change a "0" to a "1" by ultraviolet light erasure is necessary. (See article on UV Erasure.)

The CXK27C1000DQ is set to programming mode when 12.75V is applied to Vpp pin and "L" level to \overline{CE} and \overline{PGM} .

High Speed Programming Method

During programming and verify operation a circuit that automatically monitors the programming of cells is activated. Thus over program pulse so far in use is not necessary, and programming time is greatly reduced to 13 seconds.

Program Inhibit Mode

By turning Vpp to 12.75V and \overline{CE} to V_{IH} , programming is inhibited. Using this method allows for programming of multiple devices in parallel with different data. With the exception of \overline{CE} wiring is common. With the input of $\overline{CE} = V_{IL}$ pulse into the device selected for programming, this can be performed independently from other devices.

Program Verify

To verify if programming has been correctly performed at the specified address, memory cells are read out. Data of the selected address is output by turning to $\overline{CE} = \overline{OE} = V_{IL}$, and $\overline{PGM} = V_{IH}$ at Vpp = 12.75V.

Electronic Signature Mode

Electronic signature serves to identify the manufacturer and the device type of each EPROM. This function is intended for use by the programming equipment to automatically match the device to be programmed with its corresponding programming algorithm.

At read mode, 12V is applied to address A9.

A1 to A8, A10 to A16 = $\overline{OE} = \overline{CE} = V_{IL}$ and $\overline{PGM} = V_{IH}$ is obtained.

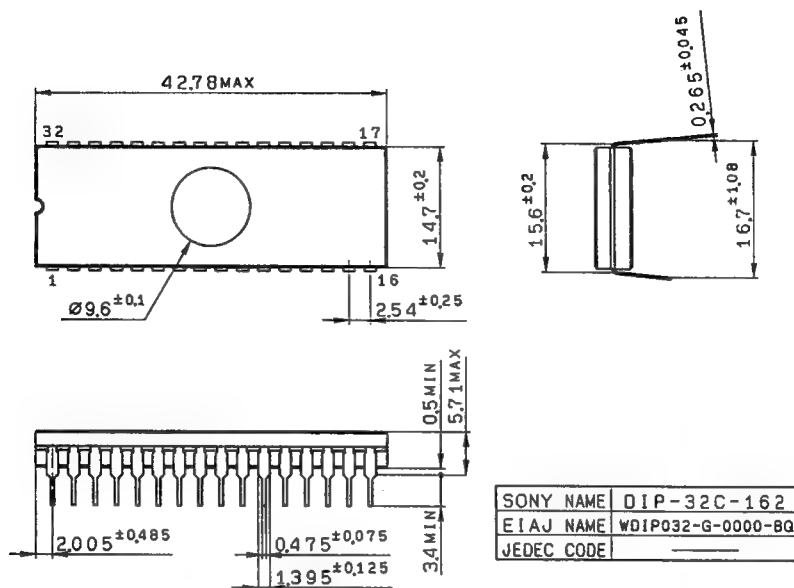
With A0 = V_{IL} the manufacturer code is output and with A0 = V_{IH} the device code is output.

The chart below shows the Electronic Signature.

Pins	A0	07	06	05	04	03	02	01	00	Hex
Signature										
Manufacturer Code	V_{IL}	0	0	1	0	0	0	0	0	20
Device Code	V_{IH}	1	0	0	0	0	1	1	0	86

Package Outline Unit : mm

32pin DIP (Ceramic)



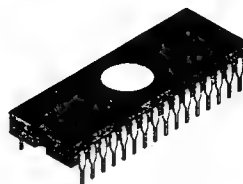
131072-word × 8-bit Ultraviolet Erasable CMOS EPROM
Description

The CXK27C1001DQ is an electrically programmable, ultraviolet erasable CMOS EPROM. The adoption of CMOS for the peripheral circuits allows for high speed operation and low power consumption. Ideally suited for 8-bit micro-processor systems requiring large program memories, this IC is organized as 131072-word by 8-bit in a 32 pin Frit-Seal package.

Features

- Fast access time : (Access time)
CXK27C1001DQ-15 150ns (Max.)
CXK27C1001DQ-20 200ns (Max.)
- Low current consumption
at operation current 50mA (Max.)
at standby 1mA (Max.)
- At read out 5V single supply operation :
5V ± 10 %
- Directory TTL compatible :
All inputs and outputs
- 3-state output
- High speed program mode
- 600-mil 32 pin ceramic DIP package

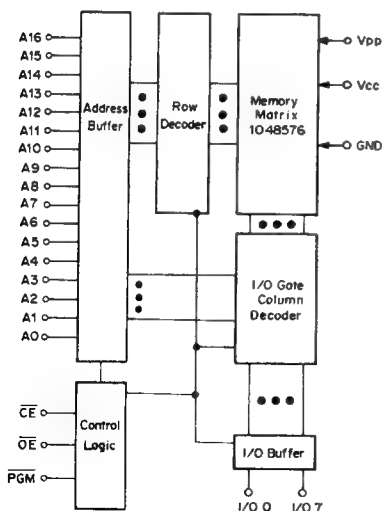
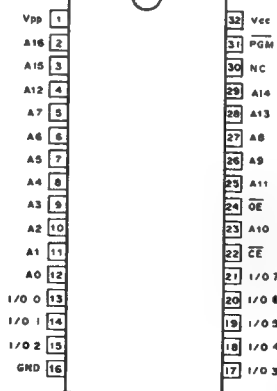
32 pin DIP (Ceramic)


Function

131072-word × 8-bit EPROM

Structure

Silicon Stacked-gate CMOS IC

Block Diagram

Pin Configuration
(Top View)

Pin Description

Symbol	Description
A0 to A16	Address input
I/O 0 to I/O 7	Data I/O
\overline{CE}	Chip enable input
\overline{OE}	Output enable input
\overline{PGM}	Program enable input
Vpp	Program power supply
Vcc	+ 5V power supply
GND	GND
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	Vcc	- 0.6 to + 7.0	V
	Vpp	- 0.6 to + 14	V
Input voltage	A9	- 0.6 to + 13.5	V
	V _{IN}	- 0.6 to + 6.5	V
Output voltage	V _{I/O}	- 0.6 to + 6.5	V
Operating temperature	Topr	- 10 to + 80	°C
Storage temperature	Tstg	- 65 to + 125	°C

Exposure to stress exceeding the Absolute Maximum Ratings may not only adversely affect reliability but at the worst, destroy the device.

Truth Table

CE	OE	A9	PGM	Vpp	Mode	I/O pin
L	L	X	X	Vcc	Read	Data output
L	H	X	X	Vcc	Output disable	High impedance
H	X	X	X	Vcc	Standby	High impedance
L	X	X	L	Vpp	Program	Data input
L	L	X	H	Vpp	Program verify	Data output
H	X	X	X	Vpp	Program inhibit	High impedance
L	L	V _H	H	Vcc	Electronic signature	Device code output

Set X to either "H" or "L", V_H = 12V ± 0.5V

Read Mode**Recommended Operating Conditions**

(Ta = 0 to + 70°C, GND = 0V, Vpp = Vcc*)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.0	—	Vcc + 0.5	V
Input low voltage	V _{IL}	- 0.1	—	0.8	V

* Vpp must be applied simultaneously or after Vcc and removed simultaneously or before Vcc.

Electrical Characteristics**• DC characteristics**

(Vcc = 5V ± 10 %, Vpp = Vcc, GND = 0V, Ta = 0 to + 70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = 5.5V	- 10	—	10	μA
Output leakage current	I _{LO}	V _{I/O} = 5.5V	- 10	—	10	μA
Vcc average operating supply current	I _{CC1}	Cycle time 125ns Duty = 100 % I _{OUT} = 0mA CE = OE = V _{IL}	—	—	50	mA
Vcc standby supply current	I _{SB}	CE = V _{IH}	—	—	1	mA
Vpp supply current	I _{PP1}		—	—	0.1	mA
Output high voltage	V _{OH}	I _{OH} = - 400 μA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.45	V

* Vcc = 5V, Ta = 25°C

I/O capacitance

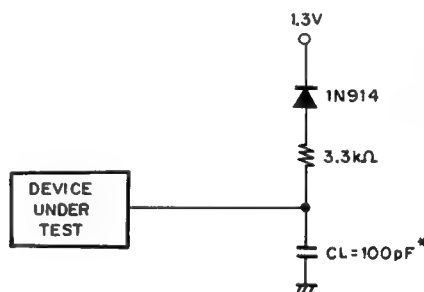
(Ta = 25°C, f = 1MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	4	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	12	pF

Note) This parameter is sampled and is not 100% tested.**AC characteristics****• AC test conditions**

(Vcc = 5V ± 10 %, Vpp = Vcc, Ta = 0 to + 70°C)

Item	Conditions
Input pulse high voltage	V _{IH} = 2.4V
Input pulse low voltage	V _{IL} = 0.45V
Input rise time	tr ≤ 20ns
Input fall time	tf ≤ 20ns
Input reference level	2V/0.8V
Output reference level	2V/0.8V
Load condition	Right figure

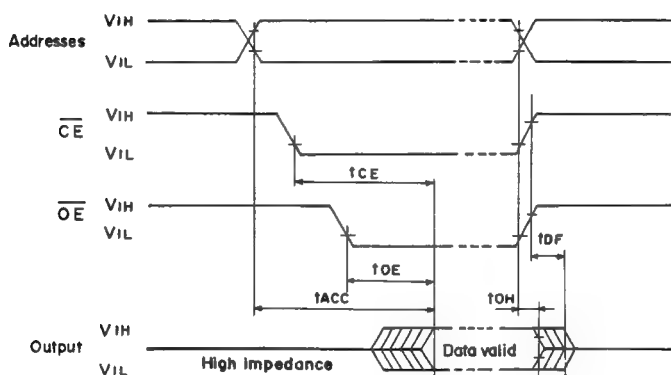


* CL includes scope and jig capacitances.

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Address access time	t_{ACC}	—	150	—	200	ns
Chip enable access time	t_{CE}	—	150	—	200	ns
Output enable access time	t_{OE}	—	65	—	70	ns
Output data hold time	t_{OH}	0	—	0	—	ns
Output disable time	t_{DF}^*	0	50	0	60	ns

* t_{DF} is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100% tested.

Timing Waveform (Read cycle)



Programming Operation**Recommended Operating Conditions**

(Ta = 25 ± 5°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Vcc supply voltage	Vcc*1	6.00	6.25	6.50	V
Vpp program supply voltage	Vpp*2	12.50	12.75	13.00	V
Input high voltage	VIH	2.0		Vcc + 0.5V	V
Input low voltage	VIL	- 0.1		0.8	V

*1 Vcc must be applied before Vpp and removed after Vpp.

*2 Keep Vpp below 14V including overshoot.

Extraction of the device while 12.75V is applied to Vpp may impair reliability.

Electrical Characteristics**• DC characteristics**

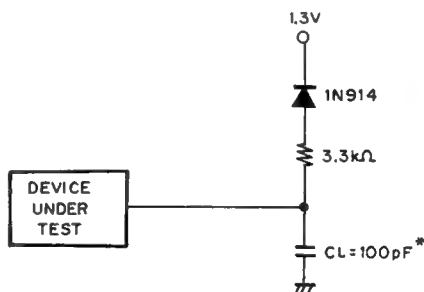
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input leakage current	II _I	V _{IN} = V _{IL} or V _{IH}	- 10	—	10	μA
Vcc supply current	Icc2		—	—	50	mA
Vpp supply current	Ipp2	$\overline{CE} = V_{IL}$	—	—	50	mA
Output high voltage (at verify)	V _{OH}	I _{OH} = - 400 μA	2.4	—	—	V
Output low voltage (at verify)	V _{OL}	I _{OL} = 2.1 mA	—	—	0.45	V
A9 electronic signature	V _{ID}		11.5	12.0	12.5	V

AC Characteristics**• AC test conditions**

(Vcc = 6.25 ± 0.25V, Vpp = 12.75 ± 0.25V, Ta = 20 to + 30°C)

Item	Conditions
Input pulse high voltage	V _{IH} = 2.4V
Input pulse low voltage	V _{IL} = 0.45V
Input rise time	tr ≤ 20ns
Input fall time	tf ≤ 20ns
Input reference level	2V/0.8V
Output reference level	2V/0.8V
Load conditions	Right figure

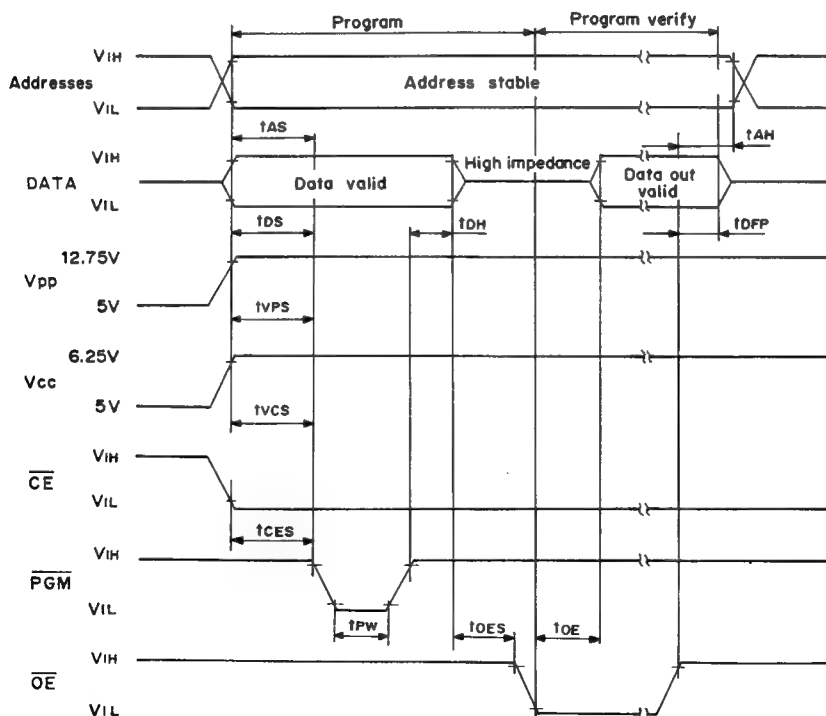
* CL includes scope and jig capacitances.



Item	Symbol	Min.	Max.	Unit
Address setup time	t _{AS}	2		μs
$\overline{\text{OE}}$ setup time	t _{OES}	2		μs
Data setup time	t _{DS}	2		μs
Address hold time	t _{AH}	0		μs
Data hold time	t _{DH}	2		μs
$\overline{\text{OE}}$ high to output float delay	t _{DFF} *	0	130	ns
V _{pp} setup time	t _{VPS}	2		μs
V _{cc} setup time	t _{VCS}	2		μs
$\overline{\text{CE}}$ setup time	t _{CES}	2		μs
Program pulse width	t _{PW}	95	105	μs
Data valid from $\overline{\text{OE}}$	t _{OE}		100	ns

* t_{DFF} is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100% tested.

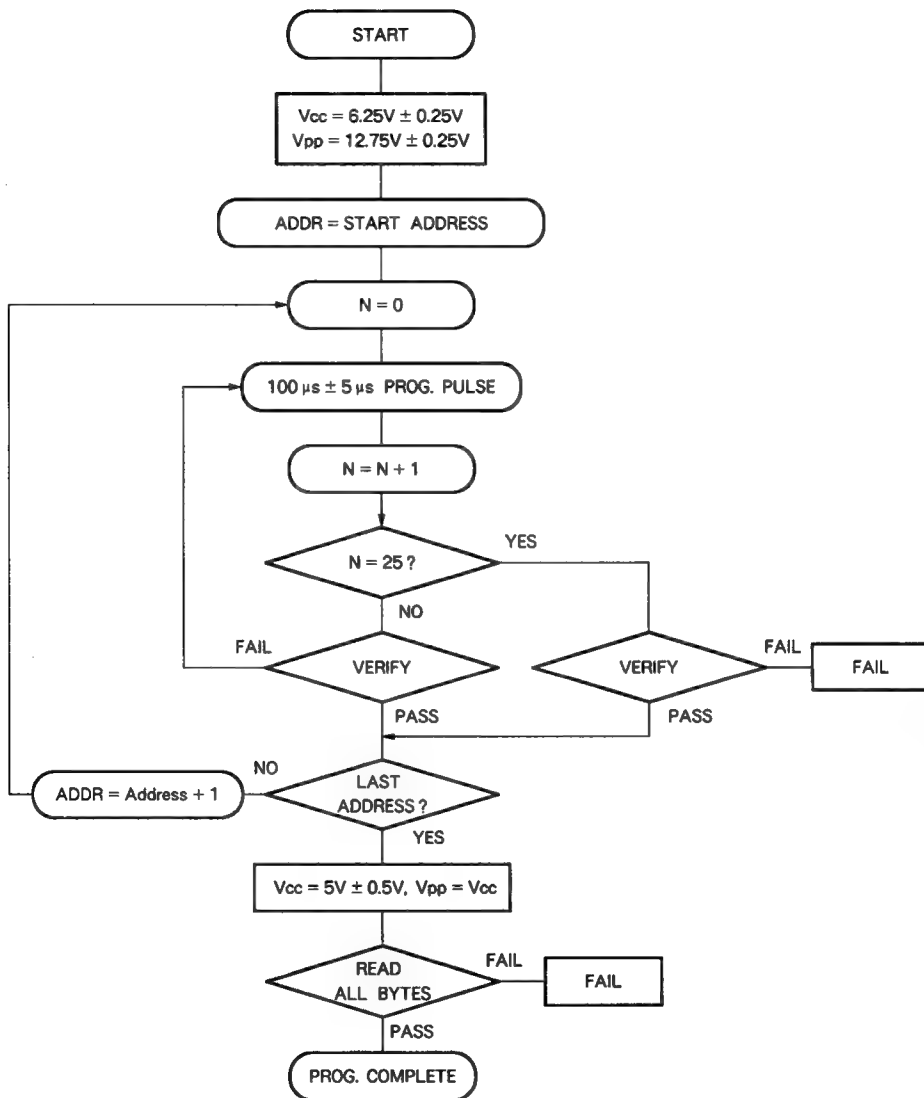
Timing Waveform (Program)



Note) When programming the CXK27C1001DQ a 0.1 μF capacitor is required across V_{pp} and GND to suppress switching noise caused by V_{pp} transient current.

High Speed Programming Method Flow Chart

Flowchart



Erasure Operation

The recommended erasure procedure for the CXK27C1001DQ ("0" to "1") is exposure to ultraviolet light of a 2537 Å wavelength through the translucent window. The exposure dose (i.e. UV intensity \times exposure time) for erasure should be at a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with an illuminance of 12000 μ W/cm² on the package surface placed within 2 to 3cm of the lamp tubes. Moreover, erasure may require larger periods according to the ultraviolet lamp life and the dirt on the quartz window.

In this IC, erasure of data starts when exposed to light with a wavelength of 4000 Å or less. Considering that sunlight and some fluorescent lighting contain elements of a wavelength between 3000 and 4000 Å, long usage under such type of lighting conditions calls for protection. In such cases, use an opaque seal and the like to cover the glass window and prevent chip exposure to light.

Operation Modes**Read Mode**

This IC features a chip enable (\overline{CE}) and an output enable (\overline{OE}). \overline{CE} selects the device and at the same time controls the power down function. \overline{OE} controls the output buffer, independently from \overline{CE} . By setting the address while $\overline{CE} = \overline{OE} = V_{IL}$, data becomes stable after t_{ACC} .

After address has become stable, respective data become stable when after t_{CE} , \overline{CE} is lowered to V_{IL} from V_{IH} in $\overline{OE} = V_{IL}$ condition, or \overline{OE} is lowered from V_{IH} to V_{IL} in $\overline{CE} = V_{IL}$ condition, after t_{OE} .

Output Disable Mode

By turning \overline{OE} to V_{IH} , the output pin turns to high impedance condition irrespectively of other inputs. This function completely prevents bus contention and allows for an easy connection of several devices on a common bus line.

Standby Mode

Turning \overline{CE} to V_{IH} automatically brings in power down condition. Then consumption current I_{CC} is reduced to a maximum 1mA. Also, output turns to high impedance condition irrespectively of \overline{OE} .

Notes on Operation

Supply current I_{CC} features 3 levels depending on the device operating condition. Standby current level, operating current level and transient peak current level. The transient peak current is the source of switching noise and the cause of high speed IC's misoperation. As the magnitude of the transient peak current heavily depends on the inductance and capacitance of the output load. This can be suppressed through the usage of a decoupling capacitor.

When the system is built, it is recommended to insert a high frequency 1 μ F ceramic capacitor between V_{CC} and GND on every device, and as close to the device as possible.

In addition, a 4.7 μ F electrolytic capacitor is recommended for every 8 devices. This should be close to the power supply to overcome voltage drop caused by the PCB wiring inductance.

Program Mode

When delivered, and after each erasure, all bits of the CXK27C1001DQ are in the "1" state (Output "H" level). Data is introduced by selectively programming "0s" (output "L" level). To change a "0" to a "1" by ultraviolet light erasure is necessary. (See article on UV Erasure.)

The CXK27C1001DQ is set to programming mode when 12.75V is applied to Vpp pin and "L" level to \overline{CE} and \overline{PGM} .

High Speed Programming Method

During programming and verify operation a circuit that automatically monitors the programming of cells is activated. Thus over program pulse so far in use is not necessary, and programming time is greatly reduced to 13 seconds.

Program Inhibit Mode

By turning Vpp to 12.75V and \overline{CE} to V_{IH} , programming is inhibited. Using this method allows for programming of multiple devices in parallel with different data. With the exception of \overline{CE} wiring is common. With the input of $\overline{CE} = V_{IL}$ pulse into the device selected for programming, this can be performed independently from other devices.

Program Verify

To verify if programming has been correctly performed at the specified address, memory cells are read out. Data of the selected address is output by turning to $\overline{CE} = \overline{OE} = V_{IL}$, and $\overline{PGM} = V_{IH}$ at Vpp = 12.75V.

Electronic Signature Mode

Electronic signature serves to identify the manufacturer and the device type of each EPROM. This function is intended for use by the programming equipment to automatically match the device to be programmed with its corresponding programming algorithm.

At read mode, 12V is applied to address A9.

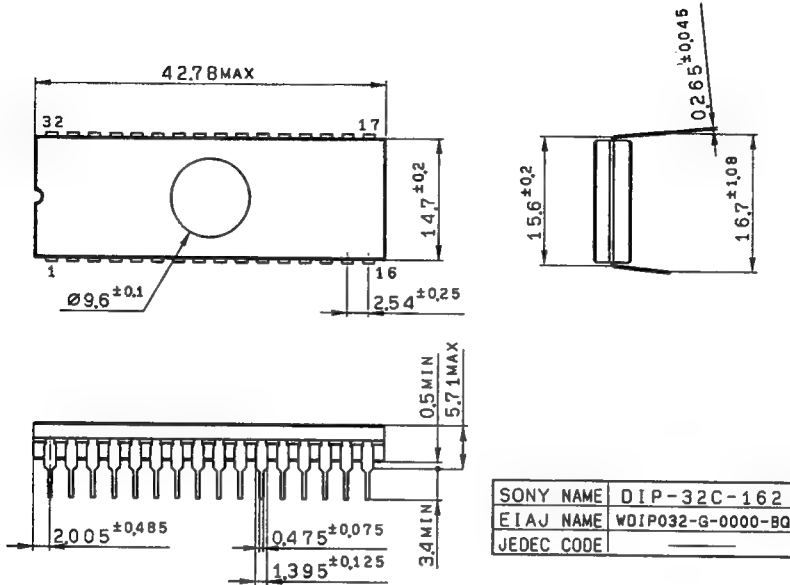
A1 to A8, A10 to A16 = $\overline{OE} = \overline{CE} = V_{IL}$ and $\overline{PGM} = V_{IH}$ is obtained.

With A0 = V_{IL} the manufacturer code is output and with A0 = V_{IH} the device code is output. The chart below shows the Electronic Signature.

Signature \ Pins	A0	07	06	05	04	03	02	01	00	Hex
Manufacturer Code	V_{IL}	0	0	1	0	0	0	0	0	20
Device Code	V_{IH}	0	0	0	0	0	1	0	1	05

Package Outline Unit : mm

32pin DIP (Ceramic)



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Sony Semiconductor Integrated Circuit Data Book

1992. Jun. 1st Edition

Edited and Published by Application Engineering Division

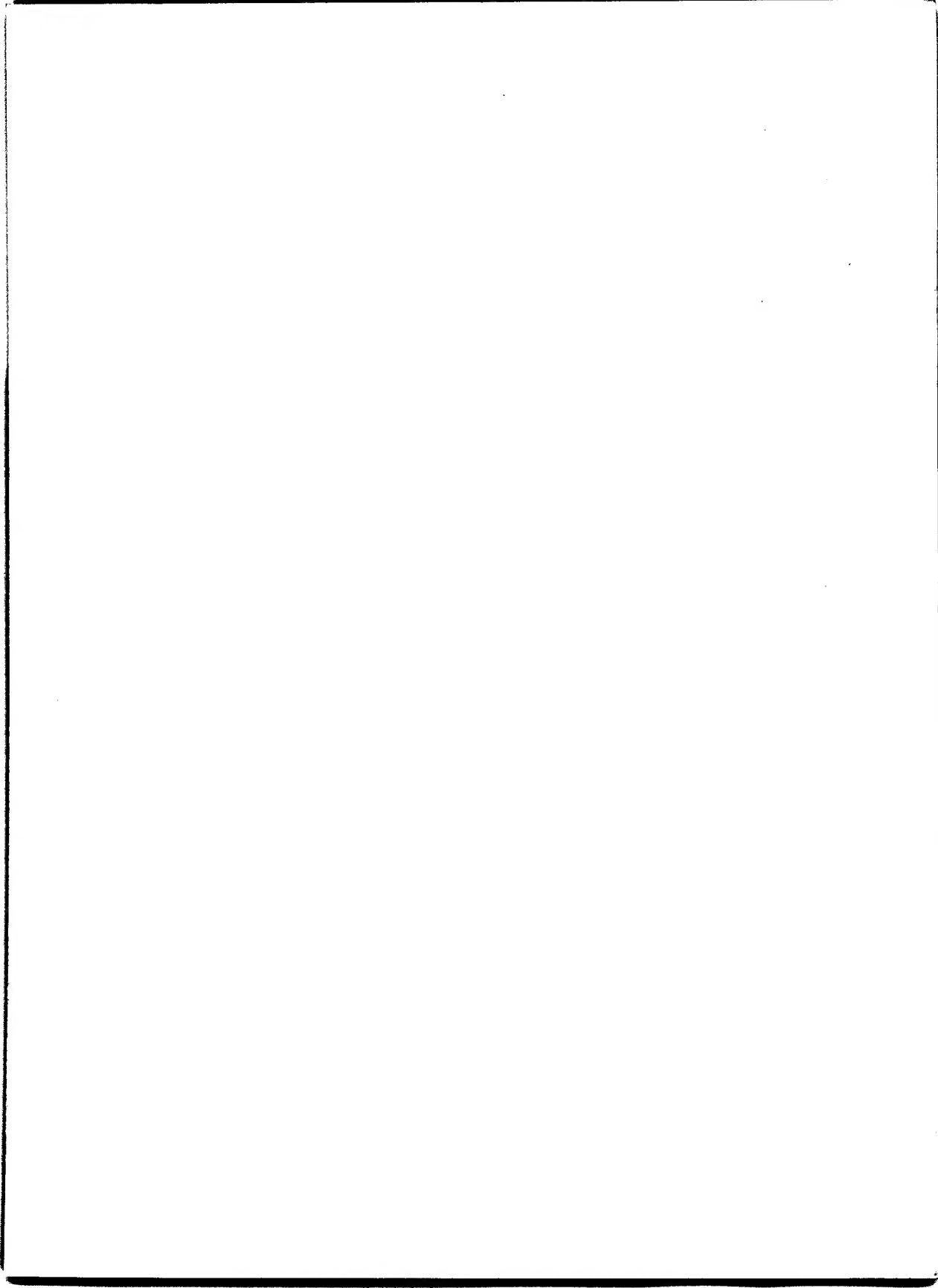
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